ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 4164

TITLE: Ion Implanted GaAs Microwave FETs

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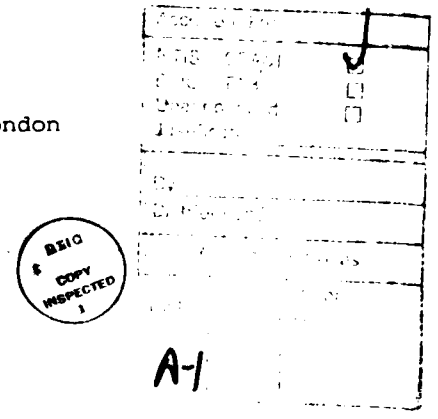
DATE: June 1988

SUMMARY

The combination of ion implantation and photolithographic patterning techniques has been applied to the fabrication of GaAs microwave FETs. This approach was adopted with the aim of providing a large number of devices having consistently predictable dc and high frequency characteristics. This memorandum concentrates on a description of the technology research carried out between 1983 and 1986 which culminated in the successful demonstration of a processing scheme meeting this objective. To validate the accuracy and repeatability of the high frequency device parameters, an X-band microwave circuit has been designed and realised. The performance of this circuit, a buffered amplifier, was very close to the design specification. The availability of a large number of reproducible, well-characterised transistors has enabled work to commence on the development of a large signal model for FETs. The preliminary work in this area is also described in this report.

As a consequence of this research programme on ion implanted GaAs FETs, considerable advances have been made in the areas of process control, dc and rf characterisation, and modelling techniques. All of these topics are important elements in future research at RSRE in microwave devices and circuits.



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1. Introduction

RSRE has been actively involved in the investigation of the gallium arsenide (GaAs) metal semiconductor field effect transistor (MESFET or FET) since the importance of this device to microwave systems was first realised in the 1970's. This research has encompassed small-signal[1], large-signal[2], and novel transistors[3]. The majority of this work relied on the use of grown layers produced by vapour phase epitaxy (VPE). This technique has been found to have two shortcomings. Firstly the uniformity of the grown layer in terms of both thickness and doping density was rather poor. Secondly the intrinsic cost of each layer was quite high. Against both criteria it has been found that ion implantation offers considerable improvements over VPE. These advantages have led to the widespread adoption of ion implantation for producing both microwave devices and in particular monolithic microwave integrated circuits (MMIC's) in GaAs.

Intramurally the fabrication of microwave transistors had extensively employed electron beam lithography for the patterning of wafers. This process is inherently slow because of its serial nature. The particular electron beam exposure system available within the Microwave Devices Division (DP2) also demanded much operator involvement because of the need for manual alignment and had only a limited slice size of 2 cm by 2 cm.

By mid 1983 it became clear that intramurally a number of factors were severely limiting progress in the area of microwave device and circuit research. The combination of VPE and electron beam lithography restricted the number of devices with potentially similar dc and rf characteristics. Extraction of dc parametric data was carried out manually from curve tracer characteristics. Rf characterisation up to this time had concentrated on high accuracy optimisation of a particular feature such as noise figure. This approach was not consistent with the need for a very reliable assessment of large numbers of devices at modest accuracy, which was required for establishing a database of rf parameters. Such information was needed to allow the extraction of equivalent circuit models of FETs, which could then be related to the dc measurements, and so aid process control.

From this appraisal of the situation a number of closely interlinked activities were launched in the Layer Processing and CAD and Circuits Sections of the Microwave Devices Division in late 1983. The major objectives of the fabrication and assessment studies are itemised in section 2, and the results of this work constitute the major part of this report. An extensive hardware and software development has been carried out to enable dc on wafer testing of devices. This topic is reported separately in RSRE Memos 4065 and 4066. In addition a new major divisional thrust on large signal modelling has been launched more recently. The preliminary findings of this work are also included in this report in section 8.

The ion implantation technology research is described in section 3. Other advances in technology and their incorporation into a whole process are described in section 4. Section 5 deals with the dc and rf characterisation techniques. These three areas of work were generally proceeding in parallel through the early phases of the study. Section 6 constitutes the major summary of the dc and rf data, which was acquired in the latter half of the programme. Section 7 describes the validation of the measurement and modelling techniques by the realisation of a buffered amplifier operating at X band.

2. Objectives

The objectives of this research programme can be subdivided into three main categories:

i) Establishment of a reproducible process for fabricating significant numbers of GaAs microwave FETs.

ii) Correlation of dc and rf properties of GaAs MESFETs realised using the reproducible and controlled fabrication process.

iii) Modelling of discrete transistors, assessing their operation in a purpose-designed amplifier, and correlating the predicted circuit behaviour with measured data.

3. Ion Implantation

3.1 GaAs Substrate Material

At the start of this work the use of un-doped semi-insulating (SI) substrates grown by the liquid encapsulated Czochralski (LEC) technique, as opposed to Cr-doped LEC wafers, was gaining favour. The reasons for this are well documented in the literature[4]. At that time RSRE was buying

GaAs off the shelf, at the mercy of the supplier to provide "good" quality material, since there was no material specification against which substrates could be bought. The first major task of this work was to identify which material properties were important and their acceptable limits. The specification for the VPE material being bought at that time for FET fabrication only quantified the doping levels and thickness of the layers (see Appendix I). The basic structure consisted of two active layers. The uppermost, or contact, layer was highly doped to ease formation of good quality ohmic contacts to the FET. The lower layer provided the conducting channel for the device.

To establish the substrate material specification involvement with the UK GaAs Consortium proved to be very fruitful, since this gave access to a specification being drawn up by the Wafer Specification Working Party. Further modifications to the draft Consortium specification and addition of other relevant information resulted in the formulation of the RSRE 2" wafer specification (Appendix II). This now forms the basis of the Device Physics Group specification for buying un-doped LEC GaAs substrates for various applications including epitaxial growth (MOCVD and MBE) and direct ion implantation. A brief justification for each of the major physical and electrical specifications is given below.

The diameter and the size of the major and minor flats are very important for all of the process steps that are computer controlled, particularly ion implantation. The orientation is defined so that the etched mesas may be oriented in the correct manner during device fabrication to ensure continuity of metal tracks running over the mesa edge, and also to control any orientation dependent effects. The sheet resistivity and the Hall mobility of carriers is specified because from these two parameters the levels of undesirable impurities (C, O, Si etc), and the electrical isolation properties (before and after an anneal cycle) can be assessed.

The so called "thermal conversion test" is carried out to ensure that the quality of the material is maintained after a dummy implant activation run (which is very similar to the MOCVD pre-clean or growth run). If the material type converts (ie becomes p-type) or becomes highly conducting, then that is a strong indication of undesirable surface effects such as impurities segregating to the surface or poor wafer polishing. This means that the activation efficiency would be very low for ion implanted devices, and poor surface morphology and interface control would be likely for epitaxially grown layers. The resistivity of the material both as supplied by the manufacturer and after the thermal conversion test was measured using a Keithley constant current source and a high input impedance (10^9 ohms) electrometer. In the cases where the material resistivity was low, the carrier

type (p or n) and the carrier mobility were measured using the Hall apparatus.

Using this qualification procedure, wafers have been procured from a number of commercial suppliers. The device data reported later was obtained from FETs fabricated on wafers from two suppliers. The ingots are referenced in the R01 and R03 parts of the wafer number. No differences in device performance could be ascribed to the use of these different sources of material. Hence this subject will not be discussed further in this report.

3.2 Ion Implantation

A new Varian 350D ion implanter was being commissioned at RSRE in the silicon processing research area at the start of this work. Therefore the early experiments had to be carried out on an older Lintott machine. This instrument had the limitation that 2" diameter (or smaller) wafers had to be attached to 3" diameter silicon wafers for mounting in the carousel. These gave many additional problems not encountered with silicon processing, mainly due to the fragility of the GaAs wafers. The Varian machine was supposed to handle GaAs wafers, both 2" and 3" diameter. However problems were also encountered here since Varian had not supplied all the special parts needed for GaAs. These were procured subsequently. After a number of breakages, the machine was eventually tuned to handle GaAs wafers (both 2" and 3" diameter) and the work progressed at a considerable pace. In the early days the implants were made into bare substrates and activated using an AsH_3 overpressure ambient furnace (see section 3.4 and figure 1). The implant conditions (dose and energy) were varied to obtain different combinations of doping level and layer thickness. In all the work for n-type doping of GaAs, the mass 29 isotope of silicon was used, as opposed to the naturally more abundant mass 28 isotope. This approach was used in order to ensure the highest purity of the ion beam, since it is well known that the mass 28 isotope can contain small amounts of for example CO (also mass 28) and other impurities. In later work a silicon nitride encapsulant was used to protect the wafer surface from contamination during the implant process. This dielectric layer was removed prior to annealing.

3.3 Theoretical Modelling

In order to produces an ion implanted layer with a similar doping profile to the VPE material used previously, the correct ion implantation conditions for ion dose and energy had to be established. The theoretically predicted Gaussian profiles, the best known being the LSS[5] theory, were used as the starting point. In figure 2 are presented the theoretically predicted atomic profiles from the implant conditions that were first used in the process. Also shown in this figure is the measured electron concentration and Hall

electron mobility as a function of depth. It is worth noting that the range (R_p) and the standard deviation (ΔR_p) were specifically calculated for GaAs rather than using the approximate numbers for Ge or Si substrates. In figure 3 is presented the theoretically predicted atomic distribution for modified implant conditions, for which allowance is also made for the fact that through nitride (40 nm thick) implants were used. In this case the PRAL[6] theoretical predictions are employed. The computer program to calculate the PRAL theoretical atomic profiles has been only available to RSRE since 1986 via the University of Surrey. In both cases the expected electron drift mobility is also plotted as predicted by Sze and Irvin[7].

3.4 Annealing

The process of ion implantation damages the host lattice and subsequent heat treatment (annealing) is required to relieve the crystal structure of implantation damage and to ensure that the dopant atoms are incorporated on appropriate substitutional sites (electrical activation). Silicon was used as the n-type dopant for all the work and generally it is well known[8] that post implantation heat treatment requires temperatures of 800 to 900°C for times of 30 to 20 minutes, respectively. The actual temperature/time cycle is also dependent on the implant dose/energy combination that is being used. GaAs evaporates congruently up to about 650°C. Above this temperature the more volatile constituent (As in this case) is lost from the surface of the semiconductor leaving behind a metallic (gallium) surface. Therefore during annealing it is essential that the loss of As is minimised.

There are two distinctly different approaches which achieve the same effect. One approach is to encapsulate the surface, for example with silicon nitride, silicon dioxide, or some other dielectric material that is stable at high temperatures. The encapsulant ensures that very few of the As atoms leave the GaAs surface, and therefore the semiconductor surface remains stoichiometric. The other approach is to ensure that there is an overpressure of As all around the GaAs surface to maintain a dynamic equilibrium, which ensures that the GaAs surface remains stoichiometric.

At the start of this work there was no dielectric deposition capability within DP2 which would serve the purpose of providing an encapsulant for ion implanted GaAs. However a redundant alkyl growth kit was available which had the gases N_2, H_2 and AsH_3 connected to it. It was decided to use AsH_3 overpressure for implant activation of half 2" diameter wafers. The AsH_3 was provided by a AsH_3/H_2 gas mixture further diluted with H_2. The furnace was characterised for temperature uniformity (figure 1) and the flow rates of H_2 and AsH_3 were also established to give 7×10^{-3} torr AsH_3 overpressure in the furnace tube. This overpressure was estimated to be that required to ensure minimal loss of As

from the surface and was also comparable with the overpressure reported in the literature[9].

Initially the anneals were carried out with the active (implanted) surface "open" to the AsH_3 gas passing over it. However it was discovered that this gave non-reproducible annealing behaviour and in some cases etching of the GaAs surface was observed. This has been reported recently by other workers[10]. At that time it was decided to perform all the anneals "face-to-face" in addition to the AsH_3 overpressure. In this situation one wafer is placed on top of another of the same size during the anneal. However it was found that it was important to ensure that the surfaces in contact were of high quality, otherwise a poor wafer could contaminate the other wafer. So the standard process became that a 2" diameter wafer would be scribed into halves, and these half wafers would be placed "face-to-face" in the furnace. This process has worked successfully for a dose range of mid 10^{12} to 10^{15} Si^{29} cm^{-2}. The standard temperature was established to be 850°C and the anneals were of 20 minutes total duration (including about 4 minutes rise time).

3.5 Electrical Assessment

Within the division the layer assessment techniques available were electrochemical profiler (the so-called POP), double mercury probe C-V, and a totally manual Hall measurement. The electrochemical profiler was not used because it had very poor resolution especially for the channel implant layer after the top contact layer had been profiled. The double mercury probe C-V technique was also discarded because again very little information about the channel layer could be obtained. It was decided to concentrate on the Hall measurements. To obtain the depth profile for the carrier concentration and carrier mobility, the Hall measurements were combined with layer stripping. This was achieved either by acid etching in $H_2SO_4:H_2O_2 + H_2O$ (1:1:125) at 30 nm/min or by anodic oxidation and stripping.

Initially the Van der Pauw samples were prepared by air abrading clover leaf shapes. However this technique can cause surface damage, wafer contamination from the materials used in the process, and the loss of samples because of the fragility of the GaAs in the clover leaf pattern. Therefore later samples were prepared exclusively by defining patterns using photoresist and etching. This process leaves a square piece of GaAs with a clover leaf pattern etched on the surface, and is consequently much easier to handle. In/Sn dot contacts to the four corners of the samples were sintered at about 300°C. After the appropriate number of differential Hall and strip measurements the step height was measured using a Dektak surface profiler (prior to the purchase of the Dektak, an interference contrast microscope was used), and the correct etch rate measured.

Figures 2 and 3 are examples of the electron concentration and Hall mobility as a function of depth. The theoretical atomic concentration profiles and the predicted mobility profiles are also shown. The peak electron concentration for the earlier layers was measured to be 1.8 x 10^{18} cm^{-3} at a depth of $\simeq$ 0.2 micron and the doping in the channel layer was $\simeq$ 4 x 10^{17} cm^{-3}. As can be seen from figure 2 the contact layer doping was much less than the theoretically predicted atomic concentration. The maximum possible incorporation of Si on substitutional sites in ion implanted GaAs at temperatures of 850°C was considered to be responsible for this maximum value of n^+ doping and was in agreement with published work[11]. In the case of the channel doping apparently higher electron concentrations than the theoretically predicted atomic levels were measured. This can be explained by the fact that all the dopant in the low dose implanted channel is activated and also impurity gradient concentration diffusion combined with radiation damage enhanced diffusion may have caused much more of Si to be present in the deeper channel layer than predicted. The deviation of the theoretical mobility curve from the experimental results indicate both non-complete recrystallization of the implanted layer and also high levels of residual impurities in the host substrate layers.

In figure 3 the electron concentration depth profile again indicates deviation from the theoretical atomic profile however a much better agreement than previously has been obtained. The PRAL[6] predictions in fact much more closely resemble the experimental atomic profiles generally. We observe that again in the channel layer higher doping levels were achieved than those theoretically predicted and we believe the explanation given above about diffusion applies in this case also. It is interesting to note the experimental and theoretical mobility profiles agree more closely, and we believe this is an indication of both better quality substrates (lower background impurities) and more complete recrystallization of the implanted layer in the later samples.

4. FET Process Research

4.1 Ion Implanted FETs

An intermediate goal of this programme was the substitution of implanted wafers for the VPE grown material used previously. These implanted wafers were processed using the standard electron-lithography process scheme in use at the start of this programme. The wafer processing sequence is outlined in appendix III. Table I compares the active layer structure and device results for both a VPE and an ion implanted wafer processed using the scheme in appendix III.

The implant conditions were selected to give a similar doping profile to that of the VPE material. In this

case the implants were made directly into bare SI-LEC GaAs. The implant conditions were 8 x 10^{12} Si^{29} cm^{-2} at 360 keV (using doubly charged ions at 180 keV because the machine limit was about 200 keV) for the channel layer, and 4 x 10^{14} Si^{29} cm^{-2} at 90 keV for the contact layer. These implants were activated using arsine overpressure furnace annealing. It can be seen from table I that in terms of basic dc parameters the ion implanted FETs were of at least comparable quality to those fabricated on VPE material. It should be noted that measurements from curve tracer characteristics had to be used to extract the dc device parameters, because the on-wafer probing facility was not available at that time. This level of performance was obtained from a number of implanted wafers processed with this electron beam lithography based patterning approach. With this basis established, the second phase of the work was commenced, namely the incorporation of photolithographic patterning to allow the acquisition of a much larger quantity of dc and ultimately rf data.

4.2 Mask Set and Device Measurements

The mask set used in this work comprised two basic elements, a test pattern and a microwave transistor. The test pattern section was copied from a mask set designed by the UK GaAs Consortium Substrate Working Party for a study of device uniformity. This mask design was laid out for the Consortium by STL, and the masks were made by RSRE. The microwave transistor was of a fairly standard design, which had been in use at RSRE for some years. It consisted of two gate fingers each nominally 1 micron by 100 micron in a 5 micron source drain gap. One pattern repeat of this layout is shown in figure 4. A 'numbers' mask was also introduced which uniquely identified each FET on the wafer and this has proved to be very important.

There are three levels to the overall mask set. The red colour is the mesa (or isolation) layer, the blue colour is the ohmic metal layer, and the green colour is the gate metal layer (see figure 4). The latter is arranged so that it overlays the ohmic metal for ease of bonding. The 'numbers' mask is normally introduced at the ohmic level for automatic probing at that stage. In figure 4 all the pads are numbered and the function of the various pads is given in detail in Appendix IV.

4.3 Process Scheme

The three main stages of the discrete device fabrication are i) mesa etching, ii) ohmic metallisation and alloying, iii) gate metallisation. The implementation of the first was fairly straight forward and very similar to the previously used process. However the second stage required a considerable amount of work. It was found that in many cases due to non-perfect exposure and development of the photoresist

pattern, a thin film of photoresist was left on the GaAs. This led to a failure of the subsequent ohmic metallisation and alloying process. For this reason the test of "scumming" was introduced into the process sheet. At the stage just prior to the deposition of the ohmic metals, the exposed pattern is checked for the presence of an active layer, step 24 in Appendix V, by manually probing and observing the I-V characteristics on a curve tracer. If the bare GaAs is probed then no obvious scratching of the surface takes place. However if a thin organic film (scum) is left on the surface, this is peeled off by the probes and is an indication of poor exposure/development.

The ohmic metals used and the method of alloying (either slow graphite strip heater or fast infra red lamps) were researched extensively and has led to a number of publications[12,13,14]. The results have also been disseminated to the UK industrial laboratories. Some fairly rudimentary problems such as the presence of gold blobs deposited at the ohmic stage were also identified and solved. The gold blobs caused problems at the gate definition stage, because the technique of virtual contact between the wafer and the photomask was used. The gold blobs caused the contact to be non-planar, which consequently meant that gate lines of various lengths from 0.5 to 2.0 micron across a wafer were obtained. This problem was overcome by taking particular care during deposition of the Au to ensure a slow heat up and subsequent evaporation of the metal source. In selecting the gate and the ohmic metal, consideration had also to be given to the fact that the next stage of the process involved bonding to the metal pads for rf testing. It is worth noting that the process scheme (Appendix V) was written so that well trained industrial staff could process the wafers with the minimum of supervision.

4.4 Photolithography

As mentioned in section 1, it was decided from the outset that photolithographic techniques should be adopted as the method of device patterning in this programme. Although this has a number of advantages, it does have the drawback that each new layout design requires a new mask set, which is both time consuming and costly to procure. The mask set used for all of this work has been described in section 4.2. Although, in principle, feature sizes of one micron are achievable using photolithography[15], such a process is difficult to control. To improve reproducibility and linewidth control, this work was carried out using a Karl-Suss MJB3 mask aligner. This equipment incorporated a filter, which allowed only deep UV light (at 365 nm, the I line of the mercury lamp) to impinge on the wafer, and so improve the resolution capabilities. Prior to this programme, minimum feature sizes of only 5 microns had been produced at RSRE with this system.

A comprehensive set of experiments was carried out to examine the effect on linewidth control of photoresist spin time, spin speed, spinner acceleration, bake temperature, drying temperature, chlorobenzene soak time, and exposure time. This work produced a basic process scheme, which has been slightly modified during the course of the work. The final version of the photolithographic patterning is given in appendix V.

5. Device Characterisation

5.1 DC Measurements

On completion of the ohmic metal alloying stage, dc data to assess the quality of the ohmic contacts was collected and analysed. A decision was then made whether to continue the processing or abandon the wafer depending on the quality of the ohmic contacts. Generally a contact resistance of less than 0.5 ohm mm was considered to be the absolute minimum requirement. At this stage only the "transmission line" data was collected, (pads 11 to 15 in figure 4), although other information such as ohmic metal resistance and isolation quality could also be measured.

After the gate metal stage the wafer was fully dc characterized. Both the FET and test pattern parameters were measured. In the wafer assessment routine, the following parameters were measured on the FETs (given in chronological order)[16, 17]:

(i) R_{slope}
(ii) I_{dsso}
(iii) g_d
(iv) V_{knee}
(v) g_m
(vi) I_{gate}
(vii) I_{dss4}
(viii) V_{pinch}

The autoprober was used to probe as many or as few devices as required. In general the tendency was to measure all the devices, and the data was logged for each and every device with its unique identification for data analysis at a later stage.

In addition the test pattern was also probed to assess the quality of ohmic contacts (50-100% testing) and to obtain a doping profile from C/V measurements on FATFETs (% variable depending on time available to measure, usually probed overnight for 100% testing). Other parameters such as gate metal resistance, ohmic metal resistance etc (see figure 4) could also be measured if desired. The full details of the measurements techniques using the automatic prober are described in references 16 and 17.

5.2 RF Measurements

At the time that this work was carried out, there was no on wafer rf testing facility within RSRE to allow S-parameter measurements in the GHz range. In addition up to 1983, no routine procedures had been established within the division to extract S-parameters for individual devices. Therefore such a procedure had to be established as part of this work. After the detailed dc assessment, the fully fabricated wafer was scribed into appropriate dies. It was then thinned from the back down to about 150 microns, and the individual devices were then separated for mounting and rf assessment. The FETs were assessed for microwave performance by measuring their S-parameters using an Automatic Network Analyser (Hewlett Packard HP8410, covering the frequency range 2-18 GHz).

About ten (sometimes more) devices from each wafer were measured. The device selection criteria were either geographical position on the wafer or based on one of the dc characteristics eg g_m, I_{dsso} etc. The bias conditions on the devices was fixed at V_{ds} = 5 V; V_{gs} = 0 V. From these measurements variations in microwave performance both across the wafer and from wafer to wafer were assessed, and any correlation between dc parameters and rf performance noted.

5.3 S-Parameter Extraction

Scattering (or S) parameters, like Z, Y, or H parameters, completely characterise any device or network. The advantage of S-parameters is that they are measured with the device under test embedded between a 50 ohm source and a 50 ohm load, and there is little chance of oscillations occurring.

The S-parameters of the device under test (figures 5 and 6) (DUT) were measured vectorially with reference to two fixed planes. These "Reference" planes were defined at each frequency by a calibration procedure, prior to measurement. The approach has been to define these reference planes as close as possible to the terminals of the FET. This has necessitated the design and construction of a jig, device carriers, and calibration pieces of sufficient quality to be used up to 18 GHz, which enable the FETs to be characterised in a microstrip environment.

The network analyser measured the network between the defined reference planes and hence, in the present case, measured the FET, bond wires, the via holes, and the dumbell shaped pad. These parasitic components have been characterised separately and can be allowed for in the measured data to give the S-parameters of the bare FET.

6. Experimental Results

6.1 Summary of Wafers Processed and Analysed

A great amount of evolutionary work took place in tuning the process. During the periods of 4Q-85 to 1Q-87, 34 half 2" diameter wafer starts were made. A total of 14 had gone through the dc testing stage, and more than half of these had gone through to the rf testing stage. About a third of the wafers were lost during processing due to mechanical failures (breakage) and the remainder lost due to poor processing (gold blobs, poor ohmics etc). It is worth noting here that the handling of small pieces of GaAs is much more difficult and more liable to mechanical failures than whole 2" diameter wafers. In these wafer starts a total of 54000 devices that had passed the dc criteria were fabricated and therefore provided a large pool of devices for the correlation work and amplifier design. In total about 150 FETs have been rf tested up to a frequency of 18 GHz. In table II is a summary of all the wafer starts with appropriate historical details such as processing time, number of working dc devices, number of devices tested at rf, and also the main causes of failure. Using the S-parameter data a number of amplifiers have been designed and the performance predicted, which was then correlated with the measured amplifier response (see section 7).

6.2 Specific Examples

6.2.1 DC Characterisation

The earliest successful half-wafer completed using the 1 micron photolithography process was during Q3 of 1985 (Wafer No 10R01B). On this first sample 1246 FETs were tested with an overall yield of 82% within the rather wide default limits. In figures 7-15 are shown the various parameters for this half wafer, in addition in figure 15 are identified the pass/fail limits of these devices. Of the more important parameters the dc gain (g_m) was measured to be 117 ($\pm$ 24) mS/mm, I_{dsso} 21.5 ($\pm$ 8.5) mA, R_{slope} 35 ($\pm$ 21) ohms, and V_{pinch} 1.1 ($\pm$ 0.3) Volts. The standard deviations were calculated using the raw data, without any screening whatsoever. This wafer was processed exactly according to process SS1 (Appendix V). It is interesting to note that this wafer was completed in 3 months exactly. The value of R_{slope} on this wafer was higher than expected, but is consistent with the lower than target I_{DSS} indicating that the wafer was overetched at the gate recess stage.

The processing turnaround time has reduced considerably since that first successful half wafer. Wafer No 38R03/B was processed in 4 weeks during March/April 86. Only a small piece of the original wafer was completed, due to the half wafer cleaving into a further two halves during processing. The dc properties of this wafer are listed in

figure 16, which also serves the purpose of showing how the data was logged for future reference. In comparison with the wafer quoted earlier the mean dc properties are g_m was 108 ($\pm$ 6) mS/mm, I_{dsso} 41 ($\pm$ 11) mA, R_{slope} 24 ($\pm$ 6) ohms, and V_{pinch} 2.5 ($\pm$ 0.6) volts. The latter three dc properties are fairly typical for the majority of the remaining wafers processed during this research, as shown in table III. This table is a compilation of the completed wafers with reasonable yield. In addition for this wafer the TLM pattern was used to measure the quality of the source/drain ohmic contacts. Standard Ge/Au ohmics were used and alloyed using the conventional graphite strip heater. The mean contact resistance was measured to be 0.23 ohm-mm (std dev 0.03 ohm-mm) which translates to a contact resistivity of 7 x 10^{-6} ohm cm^2 (12).

Additionally the option of C-V profiling of the FATFETs (L_g = 100 micron) also became available for later wafers. This gives a measure of the doping profiles on the completed devices and further helped the diagnosis of processing problems and interpretation of device characteristics. By way of an example, carrier concentration-depth profiles for 50 devices from a representative wafer are shown in figure 17 and clearly reveal the reproducibility of the doping profile. The small variation in the depth distribution is considered to be due to variation in the surface depletion region and the non-uniformity of the wet gate recess etch process.

6.2.2 RF Characterisation Results

A summary of the S-parameters at 9GHz observed for a range of selected FETs from the majority of completed wafers is shown in table IV. Between 6 and 10 devices per wafer were typically tested over the frequency range 2 to 18 GHz. The selection of devices for rf measurement was made on the basis of the dc parameters alone. The average of these values for the devices selected for rf testing is shown in table V. The S parameters show some variations, and thus reflect the fact that the process technology was still evolving particularly during the earlier phases of the work. It should be stressed that this spread is not gross, and reflects the general range still widely encountered in GaAs process tehnology. These variations are clearly illustrated in figures 18 and 19, which show plots of S_{21} against frequency for two of the earlier wafers.

From these S-parameters, an equivalent circuit for the FET can be derived from an optimiser program (LADMOP). The results from the wafers in table IV are shown in table VI. The individual parameters refer to the basic components of the equivalent circuit as presented in reference 18. It can be seen that the intrinsic transconductance derived from the rf parameters, G_m, is reasonably constant. However the C_{gs} term

shows some significant variations. This term is basically controlled by the surface doping density under the gate metal and the gate length (assuming the gate width to be constant). The consistent transconductance results would imply that the doping density under the gate is remaining approximately constant. Therefore it is reasonable to conclude that the C_{gs} variations were caused by poor control of the gate lithography.

Optical microscopy and SEM studies have confirmed these conclusions. For the earliest wafers, of which 10R01/A is typical, the gates were poorly defined and frequently resulted in a short gate length. In the next batch of wafers (37R03 and 38R03), the gate exposure was overcompensated. Gate lengths as great as 1.5 micron resulted, with correspondingly high C_{gs}. In the rf data this is reflected in the much sharper cut-off of S_{21} against frequency in figure 19 for the longer gate lengths, in comparison with figure 18. However transconductance is not strongly dependent on gate length, hence little change is observed in this parameter.

For subsequent wafers the control of gate length was improved. Mean values around 1 micron were obtained. This improved process control is reflected in generally lower C_{gs} values for wafers 02 to 05R03 and 07R03 than those observed for 37R03 and 38R03. It should be noted that the rf parameters were in general more reproducible for all of the wafers processed subsequent to 10R01/A and B. This reduced spread is attributed to obtaining a more uniform gate length across the wafer, even though the absolute magnitude changed from wafer to wafer.

The only other significant variations in table VI are in the resistance terms. In particular R_s, R_d, and R_i are lower for 10R01/A and 03R03/B. This was caused by a change in the method of optimising the fit to the S parameters for these two wafers, which were fitted at a later date than the other wafers. In general the optimiser did not seem to be very sensitive to the resistance values in the equivalent circuit, and so the other terms derived in these calculations are still deemed to be valid.

6.2.3 Theoretical Analysis

The establishment of a complete understanding of FET dc and rf performance was beyond the remit of this work programme. However some attempt has been made to analyse the observed FET performance. A simplistic view of the change in device current as a result of increasing gate voltage by 1 volt can be used to estimate the transconductance. The standard depletion calculation has been applied in this way to yield values of 87, 123, and 151 mS/mm for 1,2 and 3 x 10^{17} cm^{-3} doped channel layers respectively for a 1 micron gate length FET [19]. Typical values observed in this work lie in

the region 100 to 110 mS/mm.

A slightly more sophisticated estimate of transconductance has been derived by Engelmann and Liechti [20], which results in the relationship:

$$g_m = \frac{E_0 \, E_r \, Z_g \, v_{sat}}{d}$$

This equation relates the transconductance to the gate width (Z_g), saturated electron velocity (v_{sat}), and depletion depth (d), and yields the following values:

g_m (mS/mm)	doping density (cm^{-3})
197.8	3×10^{17}
161.5	2×10^{17}
114.2	1×10^{17}

To account for the likelihood that electrons under the gate are not travelling at the saturated velocity for the whole of the transit time, it is necessary to incorporate a two piece linear approximation to the velocity/field characteristics of GaAs. This problem was analysed by Pucel et. al. [21]. This paper provides graphical analysis of the variation of transconductance with doping density, gate length to channel depth ratio, source-drain current, and channel depth. For a channel doping of 1.5×10^{17} cm^{-3}, a gate length to channel depth ratio of 4, a source-drain current of 200mA per mm of gate width, and a channel depth of 0.25 microns, the Pucel treatment yields an estimate of 106 mS/mm.

These simple treatments yield values in the correct general range for the FETs discussed here, although they also highlight the strong dependence of transconductance on doping density. All of these calculations assume a uniform doping in the channel. In the case of ion implanted FETs, the doping is clearly not uniform (see figures 2 and 3). Furthermore the doping at the edge of the depletion region, which will dominate the transconductance around zero gate bias, would be expected to vary from wafer to wafer if the gate recess depth varies. Such variations are expected to have occurred during this work as evidenced by the range of mean source drain currents observed (table III) and the known variation in recess etch times which were employed.

A more complete analysis of FET performance can be accomplished by the use of a physical model. Such an approach allows layer doping densities, layer thicknesses, and device geometries to be provided as input parameters to a computer program. The output is a listing of key performance parameters which can then be compared with values obtained from equivalent circuit fitting to S-parameters.

A physical FET model (FETREN) has been obtained from NRL[22] for this work, and subsequently modified [23] to include recess depth and parasitic elements. The model still assumes a uniform doping profile, but nevertheless has been used to give some explanation of the observed equivalent circuit data. The values in table IV for wafers 10R01/A and 38R03/B have been taken as representing extremes of behaviour observed in this work, and have been used to assess how well the FETREN model can explain experimental data. The most highly developed program available internally was FETREN4, and this has been used to model these equivalent circuit parameters.

As noted in section 6.2.2, the variation in C_{gs} is a strong indicator of processing problems. In this fitting work, emphasis was placed on obtaining a good fit to this parameter and the transconductance. It should be noted that the transconductance obtained from rf parameters is the best comparison with the computed values, since the dc derived transconductance is an extrinsic value reduced by the presence of parasitic resistances.

Tables VII and VIII are the input and output parameters giving the best fit to the data for 38R03/B. The parameters R_{dom} and C_{dom} are related to the formation of Gunn domains, for which there are no corresponding elements in the values extracted from the S-parameters. Consequently these cannot be discussed further in this report. Good fits were obtained for the prime factors of transconductance and C_{gs}. These were achieved by making an estimate of the layer thickness from the doping profiles of figures 2 and 3, and assuming a high doping density directly under the gate. It was also necessary to input a relatively long gate length. However the transit time, tau, was not well modelled with this combination of values.

In contrast for wafer 10R01/A, it was not possible to obtain a good fit of both prime parameters. Either of these together with a good fit to the tau value could be obtained using either a high or a low value of channel doping and a short gate length of less than 1 micron.

Although the detail of this fitting work is clearly not understood, the broad findings confirm the comments made in section 6.2.2 about the effect of gate length control on device performance. They also reveal that a high doping density would seem to have been in contact with the gate metal, which can be rationalised on the basis of the data in figures 2 and 3. In general good physical models for FETs are still evolving, and are the subject of extensive research [24]. Only a relatively small amount of work has been devoted to this subject here, and it has revealed some satisfactory explanations of the observed phenomena.

7. Validation of FET S-Parameter Measurements

As a means of validating the DP2 FET S-parameter measurements a narrow band, buffered, amplifier was designed and fabricated. The design was carried out using Touchstone, a microwave CAD package. The transmission medium was microstrip on Al_2O_3. The design was kept as simple as possible and used a single open circuit stub on input and output as matching networks. The design criteria were:-

1. Centre Frequency 9.0 GHz

2. MAG $[S_{11}]$; MAG $[S_{22}] < 0.015$ at 9.0 GHz

The amplifier circuit was designed using the S-parameter data of one FET from slice 37R03/B, and optimized for this particular device. The S-parameter data of a batch of FETs from the same slice were then fed into this circuit and analysed. The selection criterion for this batch of FETs was a dc g_m of 20-25 mS. The variation in S-parameters of these FETs, mainly due to variations in gate length, led to a spread in characteristics of the model amplifier, for example the gain against frequency plots are presented in figure 20. Also the other parameter variations were:

Frequency of input match	8.6 - 9.2 GHz
Frequency of output match	8.9 - 9.1 GHz
Frequency of max. gain	8.8 - 9.2 GHz (figure 20)

Because the FET rf testing process was destructive, it was not possible to design and construct an amplifier using the same FET. It was decided therefore to use the amplifier circuit designed using data from a particular FET on wafer 37R03/B, with a FET having similar dc characteristics. This amplifier was then assessed on the ANA, the matching stubs scraped off and the FET remeasured. The data from the last measurement were then fed into the amplifier model and the results compared with the measured data on the amplifier. The agreement between predicted performance and measured performance was good, and from this plot it was estimated that the frequency of best match of both input and output agreed to better than 50 MHz (figure 21) although the magnitude of S_{11} and S_{22} differed by 30% at this frequency. Also the frequency of maximum gain of the two amplifiers agreed to better than 50 MHz and the predicted and measured values of gain agreed to within 15% (figure 21). These results were very encouraging and gave confidence in the validity of the S-parameter measurements and the Touchstone package. Since these experiments were performed, improvements have been made to the ANA calibration pieces which should enable more accurate data to be obtained leading to better agreement between predicted and actual performance of circuits.

8. Large Signal Modelling of GaAs MESFETs

8.1 Introduction

The design of circuits to operate under large signal conditions requires the use of accurate non-linear models to represent the active devices in the circuit. The primary device used in microwave circuit design is the GaAs MESFET and a process has been developed in DP2 to model these devices. A non-linear equivalent circuit is used to represent the device as shown in figure 22 and the modelling process consists of determining the values and bias dependency of each of the elements in the equivalent circuit. Several stages are involved in the process and these are described in the following sections.

8.2 Measuring Device Characteristics

Detailed dc and rf characteristics are required for each device to be modelled. The DC characteristics are currently measured automatically using an autoprober and the data is stored in a standard format on magnetic disc. The transfer characteristic of the device is measured over a wide range of gate and drain bias voltages. Having measured the dc characteristics it is possible to select bias points of interest where the I/V curves are varying most significantly with bias. About 100 bias points are currently selected. At each of these selected bias points the small-signal S-parameters of the device are measured at about 100 frequency points over the range 100 MHz to 26 GHz. An automated system has been developed based on the HP8510 network analyser which, together with various bias supplies and DVM's is controlled by a HP9836 computer. Using this system a full set of bias dependent S-parameters can be measured in about 40 minutes. In addition to the above measurements, the forward gate diode I/V characteristic and the reverse gate-drain breakdown characteristic are also measured on the auto prober.

8.3 Extraction of Equivalent Circuit Parameters

8.3.1 Current Source

In the large signal equivalent circuit, a current source is used to represent the drain-source current of the FET. The value of the current source is dependent on the intrinsic drain and gate voltages. The intrinsic voltages can be calculated from the extrinsic voltages if the values of the source and drain resistances (R_s and R_d in figure 22) are known. The expression for the current source and the values of R_s and R_d are obtained by using a curve fitting process. An expression, initially derived from physical principles is modified so as to fit the measured dc transfer characteristics of the device. A NAG library constrained gradient optimiser routine is used to perform the curve fitting operation. The result of a typical fit to measured characteristics is shown

in figure 23. The expression which gives this fit is as follows:

$$I_{ds} = I_{dss}\,(1-V_g/V_p)^{\varepsilon}.\ \mathrm{Tanh}\,(\alpha.V_d.(V_g-V_p))$$

$$V_p = V_{p0}+\gamma.V_{ds}$$

8.3.2 Fixed Elements

The elements in the equivalent circuit which are not bias dependent are the bond wire inductances, the source, drain and gate resistances and the drain source capacitance (C_{ds}), together with various parasitics associated with the physical mounting of the FET. The values of all these elements except C_{ds} are obtained by fitting the S-parameter data measured under zero drain bias conditions, to a simplified model of a zero bias FET. The value of C_{ds} is obtained by fitting the S-parameters measured at I_{dss} to a full small signal equivalent circuit, having previously fixed the bond wires and terminal resistances.

8.3.3 Non-Linear Elements

The non-linear elements in the equivalent circuit consist of C_{gs}, R_{gd}, R_i and J_{ds} together with the Schottky diode characteristics of the gate-source and gate-drain junctions. Having fixed the values of the parasitic elements as described above, each set of measured S-parameters is fitted to a small-signal equivalent circuit which then represents the FET at a particular bias point. The values of each of the rf non-linear elements can then be plotted as a function of the gate and drain bias voltages. Having obtained the values of these bias dependent elements at several discrete bias points a mechanism is required that can be used to predict the element values in the model at any arbitrary bias point. There are two alternative approaches to implementing this mechanism. An expression can be developed and fitted to the data which, provided a reasonably good fit is obtained, can be used in the model to represent the value of the device at any bias. This method has the advantage of producing a model which is easy and quick to use in a circuit analysis program; it does however take a great deal of time to develop a sufficiently accurate expression to model each new FET. An alternative approach to predicting the non-linear element values in the model is to produce a large table of regularly spaced data to represent the values at linearly spaced intervals of bias voltage. A bivariate interpolation formula can then be used to predict the element values at arbitrary points. The table can be produced from the initial fitted data using a surface fitting algorithm. This process can be implemented relatively quickly and is likely to yield more accurate results than using a functional form. There is a slight overhead in computational time however when it comes to analysing a circuit containing such a model.

The gate-drain and gate-source diode characteristics are obtained by fitting a diode I/V expression to the measured forward and reverse dc I/V data.

8.3.4 Transconductance and Output Conductance

The transconductance and output conductance of a FET can be determined by differentiation of the expression for the current source J_{ds}. The transconductance is usually independent of frequency and in the case of FET 04R05/4114 close agreement was obtained between the values of G_m obtained from the dc fit and those obtained from the S-parameter data. The output conductance however is frequency dependent and appears to change quite significantly at a frequency of about 100 kHz or less. This effect can be simulated in the model by putting a frequency dependent conductance in parallel with the current source J_{ds} and setting the transition frequency to about 100 kHz. The value of this conductance above 100 KHz is determined by subtracting the dc output conductance from the rf output conductance.

8.3.5 Using and Validating the Model

Having derived an equivalent circuit type model in which the element values are either fixed or represented by expressions or look up tables, a circuit analysis program is required which can make use of such a model. The circuit simulator ASTEC3 is currently being used and it is relatively easy to put complicated non-linear models into this program. Experiments are currently being designed to test the validity of the model, and it has already been shown that the model can accurately predict the s-parameters of the FET at an arbitrary bias point provided that the functional forms used to represent the element values are accurately fitted to the measured data.

9 Summary and Conclusions

As a consequence of the work described in this memorandum, an extensive database of dc and rf parameters has been accumulated for ion implanted GaAs MESFETs. In the course of this work, considerable advances have been made in a wide range of topics of considerable importance to the future programmes of the Microwave Devices Division.

Extensive use has been made of the division's dc on wafer characterisation facility. This has been an essential tool in diagnosing process problems, and in selecting devices for rf testing. Rigorous rf testing procedures have been established, which now reliably provide accurate information on the intrinsic device performance. Finally process control of ohmic contact formation and photolithographic gate patterning in particular has been considerably improved. In this latter area, it is perceived that further improvements in control will only be achieved by processing whole 2inch

diameter wafers, which eases the handling problems and provides more uniform flow of photoresist over the wafer surface.

Validation of the rf measurements and modelling has been accomplished by the design of a buffered amplifier. The confidence gained has allowed work to commence on developing a large signal model for FETs, which is essential for the design of non-linear circuits. Such circuits are fundamental building blocks, which could be incorporated in a wide range of future MOD systems.

Some correlation between dc and rf performance has been obtained. In particular the effect of gate length and doping density on equivalent circuit parameters has been noted. A full analysis of this area represents a very extensive programme of research, and is now being addressed by industrial laboratories, in part under extramural funding from MOD. At the start of this work, there was a need to complement the industrial research with intramural studies. However as the work progressed it became clear that extra investment from the UK companies had accelerated the pace of the extramural programmes. Therefore the emphasis of this intramural research changed. The essential features became the need to establish the basic enabling techniques as mentioned above, and to concentrate the microwave effort on an area not receiving such significant attention extramurally, namely the area of non-linear modelling.

It can be seen from these concluding remarks that two of the prime objectives of this work have been completed, and the third addressed in part. This work has provided a cornerstone on which to base the major microwave modelling and circuit design initiative in the division on large signal modelling, and also provided the necessary intramural expertise to launch an initiative on next generation microwave components.

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Table I

Epitaxial (VPE) Ref FET9		Ion Implanted Ref IMPFET1	
Contact		Contact	
doping	1.5×10^{18} cm^{-3}	doping	1.8×10^{18} cm^{-3}
thickness	0.29 micron	thickness	0.15 micron
Channel		Channel	
doping	1.6×10^{17} cm^{-3}	doping	4×10^{17} cm^{-3}
thickness	0.35 micron	thickness	0.3 micron
substrate	(Buffer/SI)	LEC-undoped SI	
g_m		g_m	
mean	99 mS/mm	mean	107 mS/mm
std. dev.	4 mS/mm	std. dev.	6 mS/mm
I_{dsso}		I_{dsso}	
mean	21 mA	mean	26 mA
std. dev.	12 mA	std. dev.	4 mA
device number	42	devices number	35
yield	90%	yield	60%

All devices Lg = 0.8 micron, S/D separation 5 micron, Wg = 200 micron.

Note All dc data obtained from curve tracer measurements, - with accuracy of $\pm$ 2 mA for I_{dsso} and $\pm$ 2 mS/mm for g_m. All electron lithography process.

Table II Historical record of processed half wafers.

Wafer No.	Start	Finish	Processed by	No. of dc tested	No. of rf tested	Comments
07 R01/A	8/11/85	20/12/85	EGB	-	-	Poor ohmics
07 R01/B	Nov '85	13/01/87	EGB	-	-	Au blobs
08 R01/A	8/01/86	31/01/86	EGB	-	-	Au blobs
08 R01/B	8/01/86	28/02/86	EGB	-	-	Broken gate stage
09 R01/A	22/01/86	12/02/86	JRD	TLM	-	Broken gate stage
09 R01/B	22/01/86	10/02/86	JRD	TLM	-	Abandon gate stage
10 R01/A	30/08/85	16/09/85	EGB	1087	13	Six bits
10 R01/B	27/08/85	13/11/85	EGB	1026	-	Small bit
11 R01/A	27/09/85	11/12/85	EGB	-	-	Non-ohmic
11 R01/B	27/09/85	18/11/85	EGB	-	-	Non-ohmic
22 R01/A	26/02/86	20/03/86	NH	267	12	Laser vias expts.
32 R01/B	11/02/86	17/02/86	JRD	-	-	Poor ohmics/broken
33 R01/A	04/02/86	12/03/86	EGB	-	-	Poor ohmic exposure
33 R01/B	03/03/86	24/03/86	EGB	86	-	Low overall yield
34 R01/A	13/03/86	13/03/86	EGB	-	-	Broken on spinner. Mesa stage.
34 R01/B	13/03/86	15/04/86	EGB	160	-	Used for ashing expts. 26% yield.
35 R01/A	17/03/86	20/03/86	EGB	-	-	Broken on spinner. Mesa stage.

Table II (continued)

Wafer No.	Start	Finish	Processed by	No. of dc tested	No. of rf tested	Comments
35 R01/B	17/03/86	15/04/86	EGB	-	-	Ammonia etched conducting layer.
36 R01/A	01/04/86	10/04/86	EGB	-	-	Ammonia etched conducting layer.
36 R01/B	01/04/86	10/04/86	EGB	-	-	Etched conducting layer by accident.
02 R03/A	15/04/86	24/08/86	EGB	150	20	Laser via expts.
02 R03/B	15/04/86	08/09/86	EGB	24	-	gd fails. 2% yield.
03 R03/A	17/04/86	01/07/86	EGB	TLM	-	Not etching gate recess
03 R03/B	17/04/86	18/09/86	EGB	202	10	27% dc yield
04 R03/A	13/06/86	15/07/86	JRD	173	19	Small piece
04 R03/B	13/06/86	19/06/86	JRD	-	-	Non-ohmic
05 R03/A	08/07/86	15/07/86	EGB	-	-	Non-ohmic
05 R03/B	08/07/86	23/07/86	EGB	257	13	Laser via expts.
07 R03/B	22/09/86	19/02/87	NH	44	-	Low yield
37/R03/A	19/02/86	14/03/86	JRD	320	12	
37 R03/B	19/02/86	14/03/86	JRD	140	18	Detailed I-V
38 R03/A	03/02/86	06/03/86	EGB	-	-	Mesa wrong way round
38 R03/B	06/03/86	01/04/86	EGB	546	13	
32 R01/A	11/02/86	19/02/86	JRD	-	-	Au blobs

Table III Compilation of mean dc values for microwave FETs on completed wafers.

Wafer No.	R_s (ohms)	I_{dsso} (mA)	g_d (mS)	V_{knee} (volts)	g_m (mS)	I_{gate} (10^{-6}A)	I_{dss4} (mA)	V_p (volts)
10R01/A	50	40	N/A	N/A	19	1.2	20	0.8
10R01/B	30	21	1	0.7	23	2	1	1.1
22R01/A	13	60	0.7	0.8	21	0.8	10	2.4
34R01/B	90	20	0.6	0.7	12	0.2	4	1.1
02R03/A1	30	30	0.8	0.6	17	0.03	8	1.4
02R03/A2	12	60	0.9	0.8	21	0.2	12	3.0
03R03/B	20	70	0.8	1.0	21	0.6	10	3.1
04R03/A	20	50	0.4	0.8	22	3	1	2.6
05R03/B	30	30	1.4	0.7	19	0.07	1	1.9
07R03/B	20	70	0.7	1.0	18	4	20	2.7
37R03/A	20	50	1.2	0.8	24	1	0.07	2.5
37R03/B	20	50	0.9	0.8	26	2	0.03	2.6
38R03/B	24	50	1.9	0.9	22	1	0.9	2.5

Table IV Summary of measured S parameters at 9GHz on selected FETs from completed wafers.

Wafer No.	Magnitude (dB)				Phase (deg)			
	S_{11}	S_{12}	S_{21}	S_{22}	S_{11}	S_{12}	S_{21}	S_{22}
10R01/A	0.61	0.06	1.8	0.66	-110	48	65	-47
10R01/B	----- not measured -----							
22R01/A	0.50	0.051	1.72	0.78	-140	73	48	-43
34R01/B	----- not measured -----							
02R03/A1	0.56	0.037	1.55	0.78	-128	78	59	-46
02R03/A2	0.61	0.035	1.50	0.79	-140	88	55	-48
03R03/B	0.60	0.037	1.34	0.86	-150	114	48	-48
04R03/A	0.50	0.048	1.61	0.77	-140	61	46	-45
05R03/B	0.70	0.016	1.43	0.74	-99	60	73	-46
07R03/	----- not measured -----							
37R03/A	0.51	0.047	1.4	0.80	-150	90	47	-45
37R03/B	0.5	0.05	1.4	0.81	-160	90	42	-44
38R03/B	0.54	0.051	1.3	0.78	-160	63	46	-46

Table V **Average dc data for microwave FETs tested at rf.**

Wafer No.	R_s (ohms)	I_{dsso} (mA)	g_d (mS)	V_{knee} (volts)	g_m (mS)	I_{gate} (10^{-6}A)	I_{dss4} (mA)	V_p (volts)
10R01/A	61	18	N/A	N/A	25	0.9	0.3	0 7
10R01/B	----- none measured at rf -----							
22R01/A	17.2	43	0.22	0.73	23.7	0.4	0.003	2.5
34R01/B	----- none measured at rf -----							
02R03/A1	23	30	0.5	0.62	20.9	0.04	0.2	2.3
02R03/A2	17.9	42	0.6	0.71	23.4	0.038	0.003	2.6
03R03/B	17.4	59.5	0.5	1.00	22.4	0.12	0.62	3.9
04R03/A	18	46	0.1	0.81	23.5	3	0.02	2.9
05R03/B	15	36	0.6	0.5	22	0.10	0.04	2.5
07R03/B	----- none measured at rf -----							
37R03/A	23	40	1.2	0.74	24	0.7	0.02	2.4
37R03/B	17	47	0.8	0.77	26.7	1.2	0.008	2.6
38R03/B	26	36	1.9	0.81	21.9	0.8	0.02	2.3

Table VI Average equivalent circuit elements derived from S parameters.

Wafer No.	L_g (nH)	R_g (ohm)	C_{gs} (pF)	R_i (ohm)	C_{gd} (ff)	G_m (mS)	tau (psec)	C_{ds} (pF)	R_{ds} (ohms)	R_d (ohm)	L_d (nH)	R_s (ohm)	L_s (nH)
10R01/A	0.6	1.08	0.26	6	20	29	5.8	0.068	340	2.8	0.4	2.8	0.09
10R01/B	----- not measured -----												
22R01/A	0.57	0.051	0.35	15	15	30	9	0.113	500	11.3	0.24	8.1	0.104
34R01/B	----- not measured												
02R03/A1	0.46	0.05	0.38	11.3	16	28.4	5.5	0.125	570	11.4	0.21	8	0.088
02R03/A2	0.41	0.05	0.45	7.7	11.9	29	6.5	0.130	700	10.6	0.24	7.4	0.073
03R03/B	0.45	1.08	0.42	6.8	6	22.7	7.9	0.081	1100	2.0	0.31	1.72	0.078
04R03/A	0.52	0.051	0.41	14	17	30	8	0.12	640	11.3	0.23	9.2	0.098
05R03/B	0.28	0.05	0.31	8.2	12	23	6.4	0.13	510	11.0	0.25	6	0.080
07R03/B	----- not measured -----												
37R03/A	0.51	0.05	0.45	13	13	26	7.2	0.122	680	10.1	0.25	10	0.088
37R03/B	0.47	0.05	0.62	8	12.9	32	7.2	0.155	710	9.4	0.29	9	0.081
38R03/B	0.49	0.05	0.52	10	17	28	7.0	0.116	620	10.0	0.27	9.7	0.081

Table VII Input parameters for FETREN4 to give best fit to experimental data for wafer 38 R03/B

Total layer thickness (micron)	0.35
Contact layer thickness (micron	0.15
Gate recess depth (micron)	0.25
Contact layer doping (cm^{-3})	1.25×10^{18}
Channel layer doping (cm^{-3})	5.00×10^{17}
Source electrode length (micron)	177.0
Source - gate spacing (micron)	1.7
Gate length (micron)	1.2
Gate - drain spacing (micron)	36.0
Gate recess length (micron)	1.4
Gate width (micron)	200.0
Gate metal thickness (micron)	0.73
Gate source voltage (volts)	0.0
Drain source voltage (volts)	5.0
Substrate current factor	4.0
High field saturated velocity (m/s)	8.0×10^{4}
Region II voltage drop factor	3.0
Fixed capacitance contribution	1.56
Gunn domain critical doping (cm^{-3})	3.0×10^{15}
GaAs dielectric constant	12.9
Threshold field (kV/cm)	3.9
Low field mobility ($m^2V^{-1}s^{-1}$)	0.20
Carrier tail shunt resistance (ohm)	3.9×10^{5}
Thermal resistance (K/W)	7.0×10^{4}
Ambient temperature (K)	300.0
Built-in voltage (eV)	0.70

Table VIII Output parameters from FETREN4 using input values in Table VII

Channel layer thickness (micron)	0.10
Source drain spacing (micron)	4.60
Pinch off voltage (volts)	3.5065
Saturation endex	0.1335
Inter - electrode capacitances (fF)	
Gate - drain	22.3390
Source - drain	36.8042
Source - gate	22.6512
Parasitic resistances (ohms)	
Drain resistance	1.8665
Gate resistance	0.2426
Source resistance	1.8665
I_{DS} (mA)	49.9843
G_m (mS)	25.9043
R_{ds} (ohms)	908.0862
C_{gs} (pF)	0.5484
R_i (ohms)	28.5999
C_{gd} (pE)	0.0166
R_{dom} (ohms)	5881.7824
C_{dom} (fF)	1.5628
Tau (pS)	15.8930

EPITAXIAL GaAs LAYER

CUSTOMER	OUR REF.	ORDER NO.	DATE
Dr J. WOODWARD	E71 650128	LOB/A 44445	7.2.85

LAYER NO.	STRUCTURE
X429	n+/n/HB/SI

PREPARED BY	CHECKED BY
(signature)	

Substrate No.	Conductivity Type	Dopant	Area cm^2	Carrier Density cm^{-3}	Resistivity ohm cm	Thickness μm	E.P.D cm^{-2}
CL2W35	SI	Cr	15.5		>10^7	400	

EPILAYER	BUFFER	ACTIVE	CONTACT
Conductivity Type	SI	n	n+
Dopant		S	S
Thickness (μm)	3.0	0.33	0.32
Carrier Density (cm^{-3})		1.5 E17	1.35 E18
Mobility ($cm^2 V^{-1} s^{-1}$)			
Resistance (ohm)			

NOTES.

1) The backface of the substrate is coated with ....

2) The C-U profile is attached. ✓

3) The substrate is orientated 2° off (100). ✓

4) The active layer thickness is taken at ....N/p..... from the C-U profile.

PLESSEY

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CASWELL, TOWCESTER, NORTHAMPTONSHIRE, U.K.

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APPENDIX II

GALLIUM ARSENIDE MMIC's

RSRE WAFER SPECIFICATION FOR 2" LEC UNDOPED GaAs WAFERS

	Parameter	Magnitude	Tolerance	Units
1)	Diameter	50.8	± 0.4	mm
2)	Thickness	400	± 12	μm
3)	Orientation	(100)	± 0.25	deg.
4)	Major Flat (Parallel to the long axis of a KOH etch pit on the seed face of wafer)	16	± 2	mm
5)	Minor Flat (90° Anti clockwise or clockwise from major flat when facing the seed surface, to be specified by the manufacturer)	8	± 1	mm
6)	Bow, warp (no vacuum)	20 (max)	None	μm
7)	Flatness TIR held on a vacuum chuck	10 (max)	None	μm
8)	Sheet Resistivity			
	i) before thermal conversion test	10^7(min)		ohm/□
	ii) after thermal conversion test	10^7(min)		ohm/□
9)	Mobility			
	i) before thermal conversion test	5000 (min)		$cm^2V^{-1}S^{-1}$
	ii) after thermal conversion test	3500 (min)		$cm^2V^{-1}S^{-1}$
10)	Etch pit density	10^5(max)		$/cm^2$

A five point average at: r/8, r/2 and centre on a <110> diagonal.

11) Surface finish: The polished surface is to be free from scratches, haze and "orange peel" when viewed with the naked eye. Wafers are to be free from texture and blemishes when inspected with X200 mag Nomarski microscope.

12) Edge rounding: All wafers to be edge rounded to SEMI standard for silicon.

13) Slice numbering and packaging: The wafers should be numbered in order from seed end of crystal. The wafers should be packaged in individual fluoroware containers with individual lids and each lid marked with ingot number and wafer number. Packed in clean room conditions, class 100, the seed end polished surface is to be placed face down in container and held in position with a spider clamp.

14) Thermal conversion test, is done in Arsine overpressure at 850 degrees C for 30 mins (total), either uncapped or in close proximity of another GaAs wafer (to be specified by the manufacturer).

RSRE INGOT QUALIFICATION PROCEDURE FOR 2" OR 3" UNDOPED GaAs WAFERS

Physical Inspections

1) The packaging shoould be in individual fluoroware containers and have individual lids with the ingot number and wafer number clearly indicated on a label.

2) Open in clean room conditions only. The seed end polished surface should be face down in fluoroware container and held in position using a spider clamp.

3) Flatness: The flatness is to be measured using the Solex Air Gauge (SP1), at five points on a jig both in free mode and held under vacuum. The diameter and flat lengths are measured by placing wafer on metric graph paper. Confirm diameter, major flat, minor flat.

4) Inspection: (i) naked eye, (ii) low power microscope and (iii) high power microscope. Check wafer surface for cleanliness, poor surface finish and any other visible defects. Check edge for chips, cracks, irregularities and correct edge rounding. Observe and photograph the wafer surface finish using Nomarksi interference microscope (x 80 and X 1015).

5) Wafer cleaning: Clean all wafers using the standard solvent clean of Acetone/Inhibisol/IPA and dry wafers at 140°C for 30 mins.

Assessment

6) Deposit 400Å of Si_3N_4 on whole of the 2" Ø wafer. Follow the standard photolithography procedure and leave the half of the wafer nearest to the minor flat coated with photoresist. The dividing line is to be normal to the major flat and splitting the wafer into two identical halves.

7) Deposit 3000Å of Ti on whole of the 2" wafer, and float off to leave half of wafer covered with 3400Å layer as the implant mask. Solvent clean wafer thoroughly.

8) Implant 6 x 10^{12} Si^{29}/cm^2 at ion energy of 180 keV at room temperature (SP1). Scribe and break the wafers into implanted and non-implanted halves. Break the non implanted half into two quarters.

9) The wafers then should be soaked in 50/50 (HF/H_2O) for 5 minutes to ensure all the Ti and Si_3N_4 is completely removed. The two halves of the 2" wafer are then to be placed face to face and annealed at 850°C for 30 minutes in AsH_3 overpressure. (Arsine partial pressure of 7 x 10^{-3} torr). One quarter of the non-implanted sample is to be placed on the implanted half (ie to cover one quarter section of it) and the other quarter is to be annealed open face in Arsine simultaneously.

10) The non-implanted half is to be assessed for type conversion and thermal stability. Two 5 mm x 5 mm samples are to be prepared in the same manner as for normal Hall effect measurements, but no clover leaf shapes are to be cut. These samples are to then be measured for resistance using

i) high input impedance "Keithley Electrometer"
ii) Keithley current source and high input impedance voltmeter

Sheet resistivity should be greater than 10^7 ohm/□ .
Then sheet Hall measurements are performed for resistivity and mobility and results analysed.
Sheet Hall mobility should be greater than 3500 $cm^2/V.s$.

11) The implanted half is to be assessed in five places using the mercury probe C-V profiler. Then two samples are to be prepared for sheet Hall measurements to confirm dopant activation and sheet Hall mobility (depth profile if felt necessary). Activation should be in excess of 70%.

12) The remainder of the implanted wafer can be used to fabricate 1 μm photolithography FET's using the common test pattern. The finished results are then dc analysed.

Note

RSRE wafer specification should be used as the guideline for quantification of the various parameters.

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ELECTRONLITH. FET FABRICATION

PROCESS E1 (11/04/63)

(Assuming slice characterised)

All solvents, DI water and blow guns filtered to 0.2 microns.
All DI water better than 10 M ohm.

EXAMINE SLICE WITH MICROSCOPE AFTER EVERY PROCESS STEP

1) Examine wafer using phase contrast and, if necessary, interferometer to assess surface quality and cleanliness. Take photo of complete wafer.

1a) Coat wafer with electron resist. (See page 4 of this appendix)

2) Scribe to required size (max. with existing ELM jig is 22 mm x 22 mm). Take photo of slice and mark wafer photo (step 1) to indicate where slice taken from.

3) Clean Slice

a) Acetone, 10 mins so + final spray + IPA spray
b) Inhibisol, 10 mins soak + final rinse + IPA spray
c) IPA, 10 mins soak + spray + final rinse in clean beaker of IPA
d) Transfer slice in beaker of IPA to chemical station and rinse for 10 mins in 10 M ohm DI water
e) N_2 blow dry
f) Check under microscope for cleanliness (Phase contrast mode)
g) Repeat any or all stages if necessary

NB At no time must slice be allowed to dry out before e).

3a) 10 sec overall etch to clean up surface. (Longer etch could be used at this stage to trim epilayer thickness). 10 min rise in DI water, N_2 blow dry.

3b) Coat slice with electron resist

See page 4 of this appendix.

4) Orientation Test

Using electron lith expose 200 x 200 micron area in corner of slice parallel to cleavage edge, and develop. (Alternatively a small piece taken from the corner of the slice can be used. It is essential that this piece is carefully referenced to the slice on both the wafer and slice photos from steps 1 and 2.)

Standard electron lith. bake.

Etch slice in $NaOH:H_2O_2:H_2O$ etch (see page 4 of this appendix) for 4 mins.

5) Strip Resist

Acetone at 35°C for ½ hour.
Acetone spray.
Fresh acetone at 35°C for ½ hour, IPA rinse and blow dry. Do not allow slice to dry out during process.

6) Examine 200 x 200 micron etch pit. One pair of opposite sides should be double edged (high magnification required). From this deduce orientation (ie double edges correspond to slope, single edges correspond to undercut).
Also use interferometer to measure depth of pit and hence confirm etch rate.
Note orientation on slice and wafer photos from steps (1) and (2).

7) Coat slice with electron resist

See page 4 of this appendix.

8) Expose mesa pattern using electron lith and develop

Orientate slice so that gate line will be parallel to single edges in step 6.

9) Bake Resist (See page 4 of this appendix). Next step is a deep etch.

10) Mesa etch

Dead reckoning, better to be over rather than under. Intended to get into SI substrate.
After calculated etch time rinse slice in DI water and scrape resist off one mesa with edge of scalpel blade.
Measure mesa height with interferometer - if necessary etch again, and check another mesa.

11) Strip Resist - see step (5)

Confirm mesa height. (If n or n^+ layer very thick and mesa underdone it might be possible to give slice an overall etch and salvage it but this is a last resort step).

12) Coat with electron resist and expose source and drain pads, develop

DO NOT BAKE or EXPOSE DEVELOPED SLICE TO ACETONE VAPOUR. The next stages involve float off and the resist profile must be maintained.

12a) Etch slice for 10 secs and CAREFULLY blow dry - check patterns and quickly go onto 13.

13) Ohmics

Electron beam evaporate	200Å	Ge
	1000Å	Au
boat evaporate	6000Å	Au

14) Float off

As a resist strip (step 5). Do not let slice dry out during this process. Essential to be quick over this step as quality of ohmic depends on time between metallising and alloying. Slice must however be clear of all resist traces before next step.

15) Ohmic Alloy (in nitrogen)

Ramp	Hold Temp	Time
20°C/min	50°C	2 mins
600°C/min	440°C	0 mins

Gas flow 70 on linear scale
Vacuum 700 mm.

16) Measure Ohmics

100 x 4 micron gap on 1 x 10^{17} n type typicall 15 ohms on N^+ on N typically 5-10 Ω.
I_{sats} on typical n layer 100 - 120 mA on N^+ on N 250 mA +

17) Coat with resist and expose gate lines and pads, develop

Examine gates carefully at very high magnification.

18) Gate line etch

a) To get down through any n^+ layer on slice.
b) To trim I_{sat} to required value - usually 20 - 30 mA.

Use probe gear with pulse box to reduce duty cycle to avoid overheating channel and making resist flow.
Monitor 2 or 3 devices across the slice and aim for I_{sat} in mid 40's.
(This will drop by approx 15 - 20 mA when the gate metal is put down).
THIS OPERATION IS BEST DONE IN SMALL INCREMENTS (about 15 - 20 sec MAX).

19) Gate and overlay metallising

E-Beam evaporate	Ti	750Å
	Pd or Pt	750Å
	Au	1000Å
Boat evaporate	6000Å Au	

20) Float off no need for high speed this time.

21) Test devices on DC probe gear.

22) Scribe and Break

23) RF Test

ETCH

Equal volumes of .05 N NaOH ('Presoak')
5 V H_2O_2
Etch rate 2200Å/min at room temp.

Two beakers - one with presoak only
one with equal volumes NaOH, H_2O_2.

30 secs in presoak to clean surface then transfer slice to etch solution for required time.

ELECTRON RESIST

1) Standard Mix

10% by weight, low molecular weight PMMA dissolved in MEK. (4 gms/50 ml).

2) Large wafer mix

5 gms PMMA in 50 ml Toluene.

ELECTRON RESIST DEVELOPER

3 IPA : 1 IBMK
2 mins at room temp, washed off with IPA and carefully blown dry. (1 micron resist patterns are delicate).

SPINNING ELECTRON RESIST

1) Standard size slices

5000 rpm
IPA dripped onto rotating slice
10 sec wait
1 drop of resist onto centre of rotating slice
10 secs wait
1 drop of resist onto centre of rotating slice

Resist thickness 0.9 micron

2) Large wafers

Flood stationary wafer with toluene bases resist and spin off at 5000 rpm

ELECTRON RESIST BAKE

Oven at 170°C. Slice in glass petri dish put into oven. 20 mins later turn oven off and allow to cool to 40°C before removing slice. (Slow cool required to minimise stress in resist layer.)

APPENDIX IV

PAD NUMBER	FUNCTION
1, 7	Gate metal resistance 6 μm x 860 μm stripe.
2, 3, 16	Standard FET, 1 μm x 100 μm gate central in 5 μm source-drain spacing.
4, 5, 16	FAT FET 100 μm x 150 μm gate with 4 μm gate-ohmic spacing. Can also be used for post process C-V profiling.
5, 7, 8	Orthogonal FET 1 μm x 100 μm gate central in 5 μm source-drain spacing.
6	Schottky backgate pad 100 μm x 100 μm.
7, 9	Gate stripe resistance
9, 15	Ohmic metal resistance 6 μm x 860 μm stripe.
10	Ohmic backgate pad 100 μm x 100 μm.
10, 11	Isolation test 10 μm gap.
11-15	Ohmic contact resistance and sheet resistance 'transmission line' pattern, with 5, 10, 15, 20 μm x 100 μm gaps.
11	Double sized pad for probe calibration.
14, 15	Ungated FET: 5 μm source-drain spacing.
FET	RSRE Common Source FET Two 100 μm π gates. Central in S-D = 4 μm.

PROCESS SS2

PROCESSING SCHEDULE FOR 1 μm PHOTOLITHOGRAPHY MESFET's (MESA TYPE)

Slice No:-

Processed by:-

1) Complete 2" wafers do NOT need any edge clearance processing.

2) Orientation is specified in the wafer specification so there is NO need to do orientation test.

3) Prior to using the mask, clean by spraying with Acetone followed by DI-H_2O wash and blow dry.

4) After each development check on manual prober for scumming!

5) Check exposure and development times on yellow room display board.

Date	Process	Comments
	1. Use only material that has passed the RSRE 2" wafer specification and ensure you know which face is to be processed for double sided polished wafers.	
	2. Clean the wafer by: Acetone spray) 2 mins each - minimum IPA spray) Do NOT let wafer dry at intermediate stages. DI water rinse (greater than 15 M ohm cm). Wash under running DI water. Blow Dry.	
	3. Deposit 400Å of SiN_x (with a 200°C bake for 30 mins prior to deposition).	
	4. Channel implant 7×10^{12} Si^{29} cm^{-2} at 240 keV Contact layer implant 7×10^{13} Si^{29} cm^{-2} at 90 keV. Tilt angle 7°, Rotation 22°.	
	5a. Cleave wafer normal to the major flat and renumber. Keep half wafers with implanted face up in the box.	
	5b. Remove SiN_x in HF/H_2O (50/50) by soaking for 10 mins. Activate implant using AsH_3 overpressure furnace, 850°C for 20 mins, with two halves being placed face to face.	

Slice No:-

Date	Process	Comments
OR	6. Anneal in 3" Ø furnace, at 800°C for 20 mins (total) using SiN_x encapsulants. Remove SiN_x in HF/H_2O (50/50) for 10 mins.	
	7. Check implant activation using non-destructive mercury probe C-V profiler on one of the batch, but clean the wafer thoroughly afterwards, in HCl/H_2O (50/50) at 20°C for 90 mins.	
	Alternatiely have the activation assessed using Hall and strip.	
	Check the activation using curve tracer on the two corners of the wafer.	Mesas
	8. Clean as in Step 2.	
	9. Bake at 200°C for 15 mins.	
	10. Spin photoresist for 5 secs at 5000 rpm (max. acc.).	
	11. Dry wafer at 95°C for 30 mins.	
	12. Check that the MESA's are orientated correctly for this mask set. Expose the appropriate MESA mask.	
	13. Develop pattern in 351 developer.	
	14. Bake slice at 200°C for 30 mins AND manually probe the bare GaAs to confirm the implant activation and that correct face is being processed, using the curve tracer.	
	15. Etch MESA in Ammonia/Hydrogen Peroxide (equal amounts) for 5 mins (approximate etch rate 0.12 µm/min).	
	16. Probe etched area (bare GaAs) to confirm isolation.	
	17. Plasma ash for 30 mins. Clean in 10% NH_3 for 30 seconds.	

Slice No:-

Date	Process	Comments
	18. Check MESA's for correct orientation and height (target is 0.3 to 0.8 μm) and photograph one pattern repeat.	
		Ohmics
	19. Repeat 8 to 11.	
	20. Soak in fresh Chlorobenzene for 15 mins and blow dry.	
	21. Dry wafer at 95°C for 15 mins.	
	22. Expose ohmics mask and numbers mask.	
	23. Develop pattern in 351 developer. Blow dry gently. NO bake.	
	24. Check exposed pattern on microscope and photograph a typical gap. Check the presence of active layer as in step 14.	
	25. Pre-clean the exposed pattern for 30 seconds using the 10% Ammonia solution and immediately deposit ohmic metallization.	
	Ge 200Å Au 800Å + Au 5000Å (deposit top up very slowly and carefully using the single ring Au approach).	
	26. Float off with care. Ash for 30 mins to remove organic residues.	
	27. Alloy ohmics using the Graphite Strip Heater cycle (999°C/m /20°C/m / 600°C/m / 60°C/m) (20°C /50°C / 320°C/ /360°C) (0 min / 1 min / 0 min / 0 min)	
OR	Rapid thermal processor using prog. 1. (440°C/15 sec).	
	28. Check the quality of some of the ohmics, photograph a typical pattern. The resistance in ohms across a gap should be about 2.0 x the gap size in μm.	

Slice No:-

Date	Process	Comments
	29. DC probe one set of TLM pattern using Autoprober.	
	30. Repeat 19 to 21.	Gates
	31. Expose appropriate gate mask with top-up for gate metallization.	
	32. Develop pattern in 351 developer, blow dry gently. NO bake. Check gate lines for correct length.	
	33. Check the I_{DSS} on a selection of microwave FET's and etch gate recess in a controlled manner, using fresh Ammonia/Hydrogen Peroxide etch in about 40 seconds.	
	34. Upon reaching the desire I_{DSS}, typically 30 mA (per 100 µm of gate width) stop the etching, rinse in 10% Ammonia solution for 30 seconds and immediately deposit gate metals.	
	35. Schottky gate is: Ti/Au 750/750 + 5000Å Au top up (total thickness of 6500Å).	
	36. Float off with care.	
	37. Check the gate metallization for gate length, etc., and photograph a typical device and gate metallization.	
	38. DC probe the devices using the Teledyne Autoprober, for FET, I-V and resistivity maps.	
	39. Scribe the FET's and Test Patterns into individual dies ready for thinning. DO NOT separate.	
	40. Wafer is now ready to be sent for lapping down to 150 µm. Full details of the procedure can be found in the "Process Book".	
	41. When wafer is returned from lapping, ash for 30 mins.	

Slice No:-

Date	Process	Comments
	42. Roll and stretch the thinned completed wafer into separate chips.	
	43. Complete the wafer data sheet.	

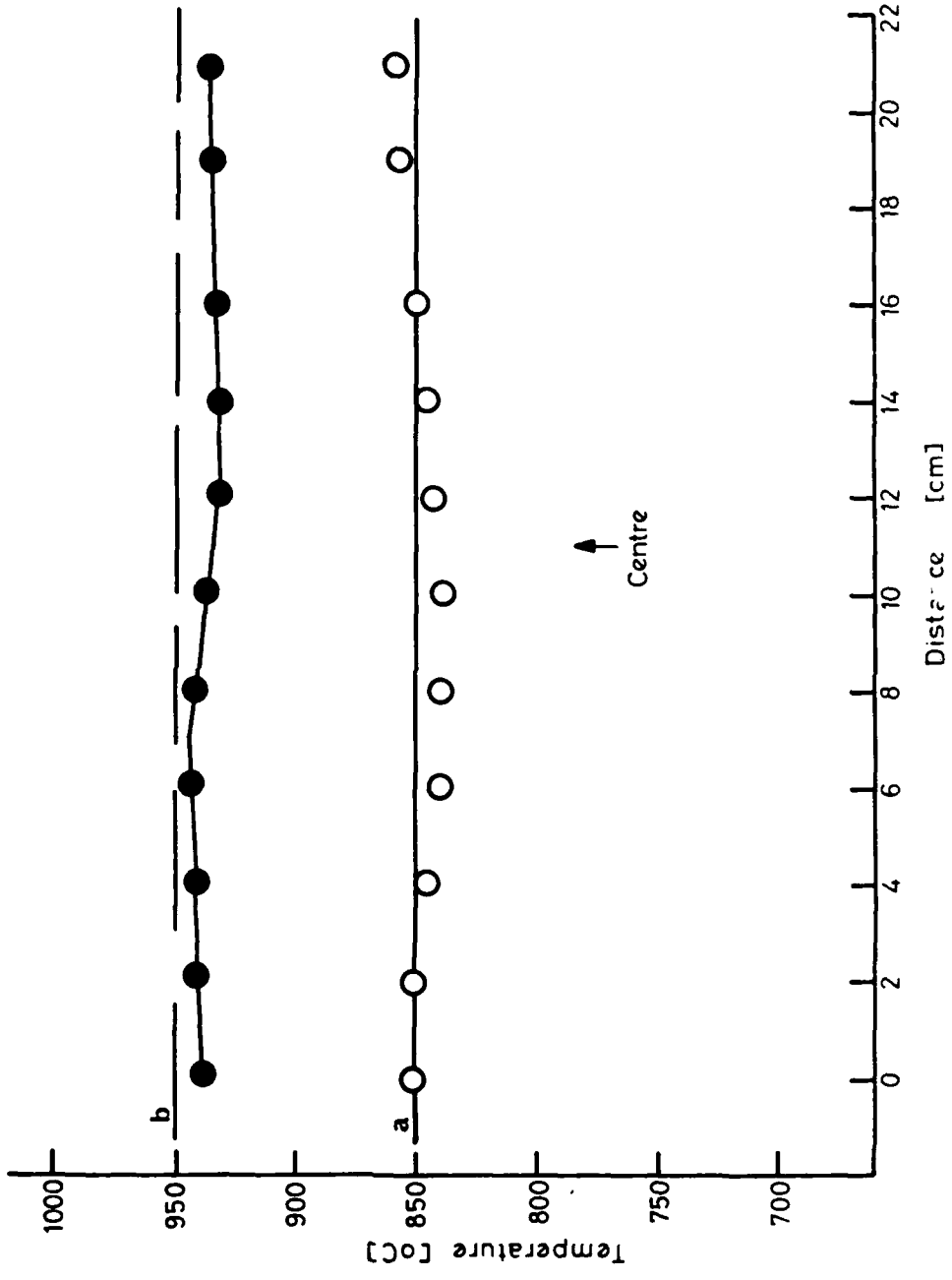


FIG 1 Temperature along furnace tube for a distance of 22 cm, for (a) 850°C, (b) 950°C.

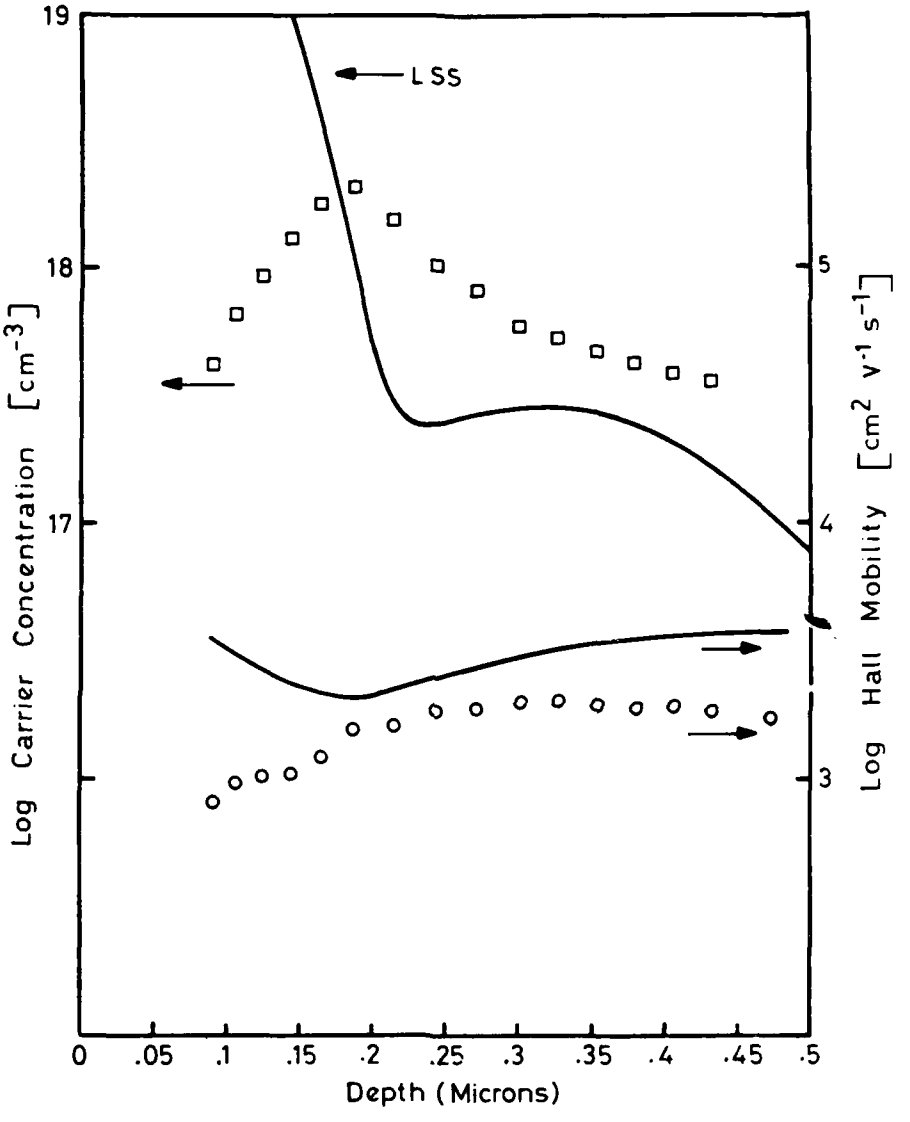


FIG 2 Electron concentration (□) and mobility (○) depth profiles for 8E12 cm^{-2}, 360 keV and 4E14 cm^{-2}, 90 keV, bare implants, annealed at 850°C for 20 minutes in AsH_3 overpressure. The calculated carrier concentration (LSS) and mobility profiles are also shown.

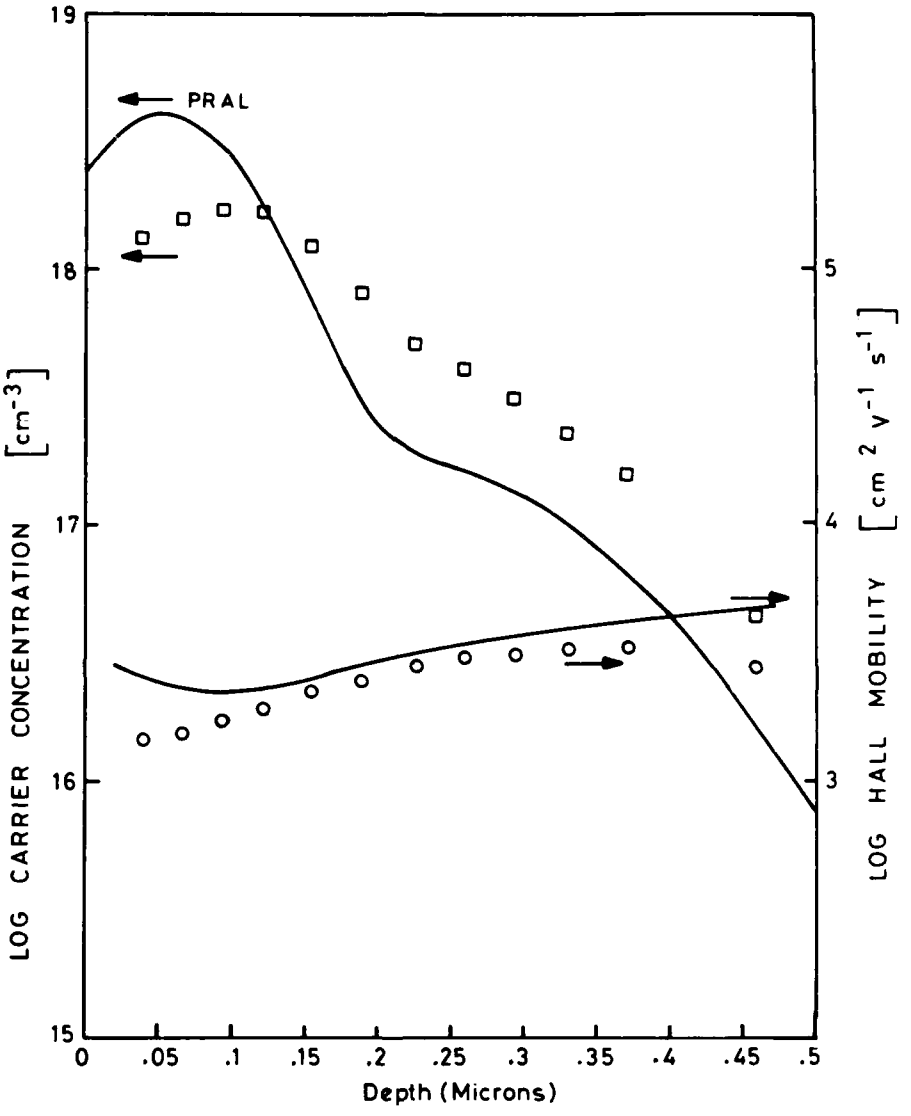


FIG 3 Electron concentration (□) and mobility (○) depth profiles for 8E12 cm^{-2}, 240 keV and 5E13 cm^{-2}, 90 keV through 400 A SiN_x implants, annealed at 850°C for 20 minutes in AsH_3 overpressure. The calculated carrier concentration (PRAL) and mobility profiles are also shown.

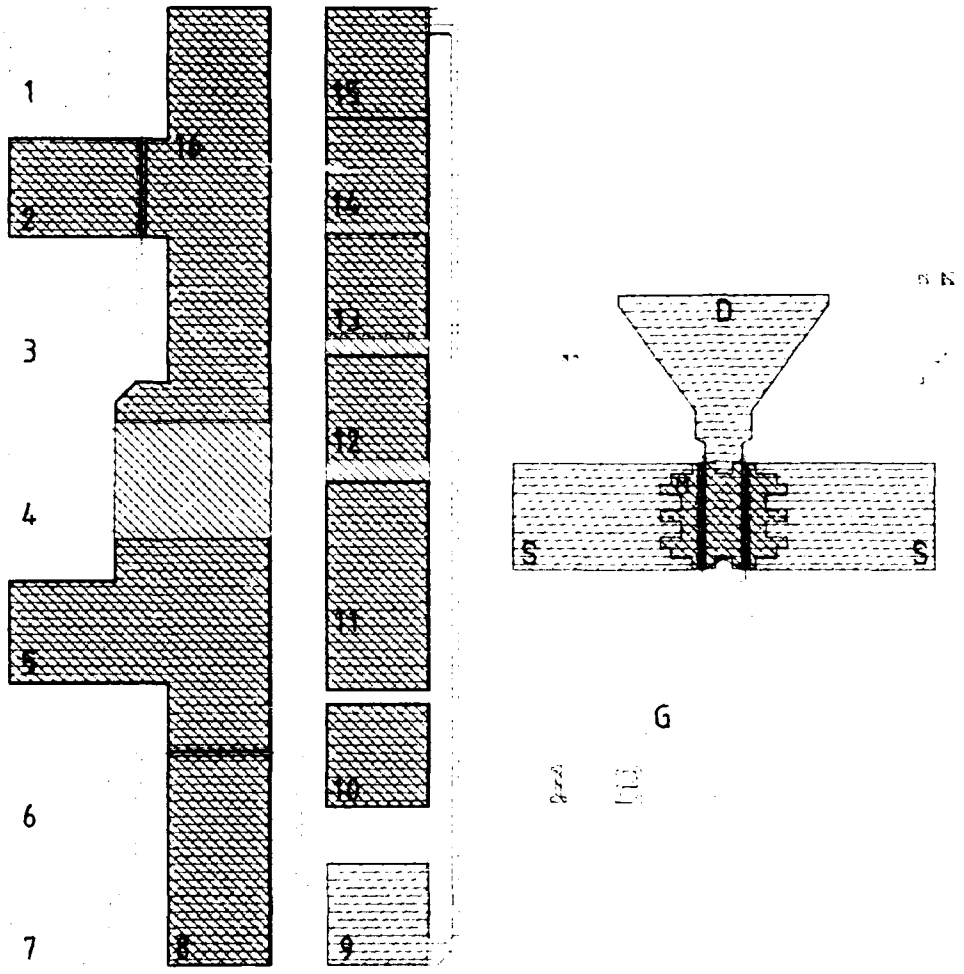


FIG 4 THE TEST PATTERN AND MICROWAVE TRANSISTOR MASK SET.
3 LEVELS OF MASKS WERE USED:
(1) RED, MESA. (2) BLUE, OHMICS. (3) GREEN, GATE PLUS TOP UP.

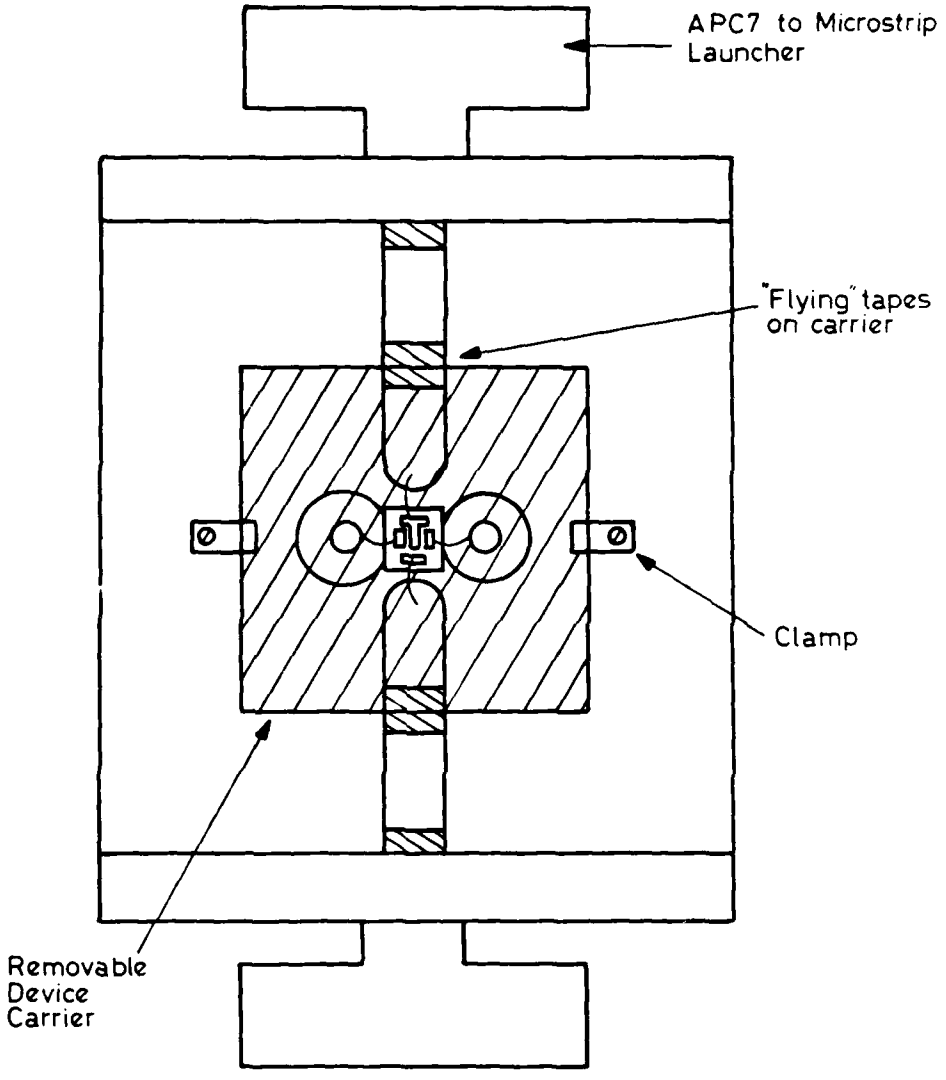


FIG 5 Device carrier mounted in DP2 A.N.A. jig for microwave characterisation.

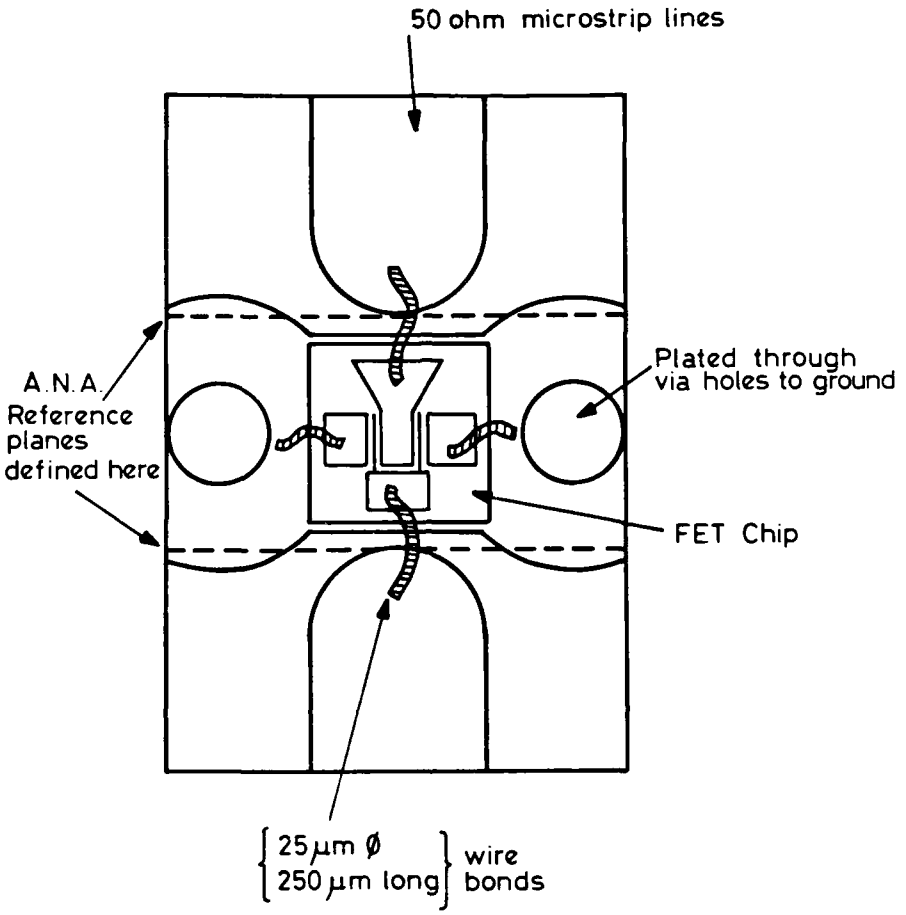


FIG 6 Details of FET mounting arrangement on device carrier for microwave characterisation.

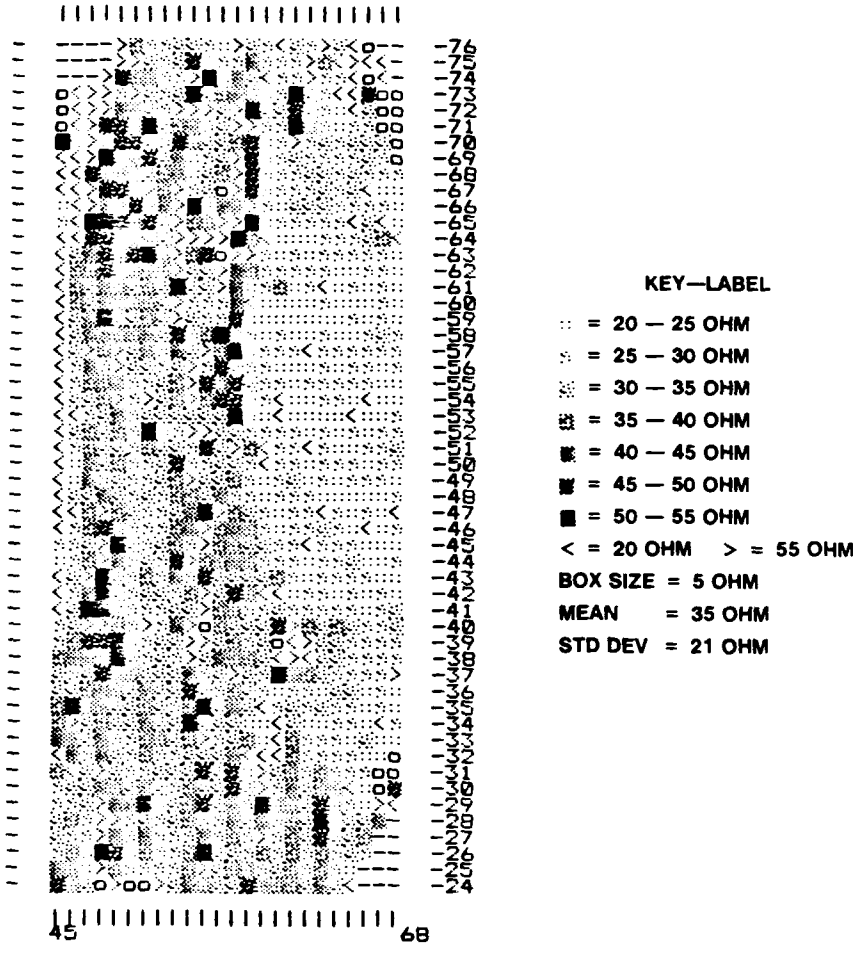


FIG 7 Map of low field resistance in range of 20 to 55 ohms for wafer 10 RO1/B.

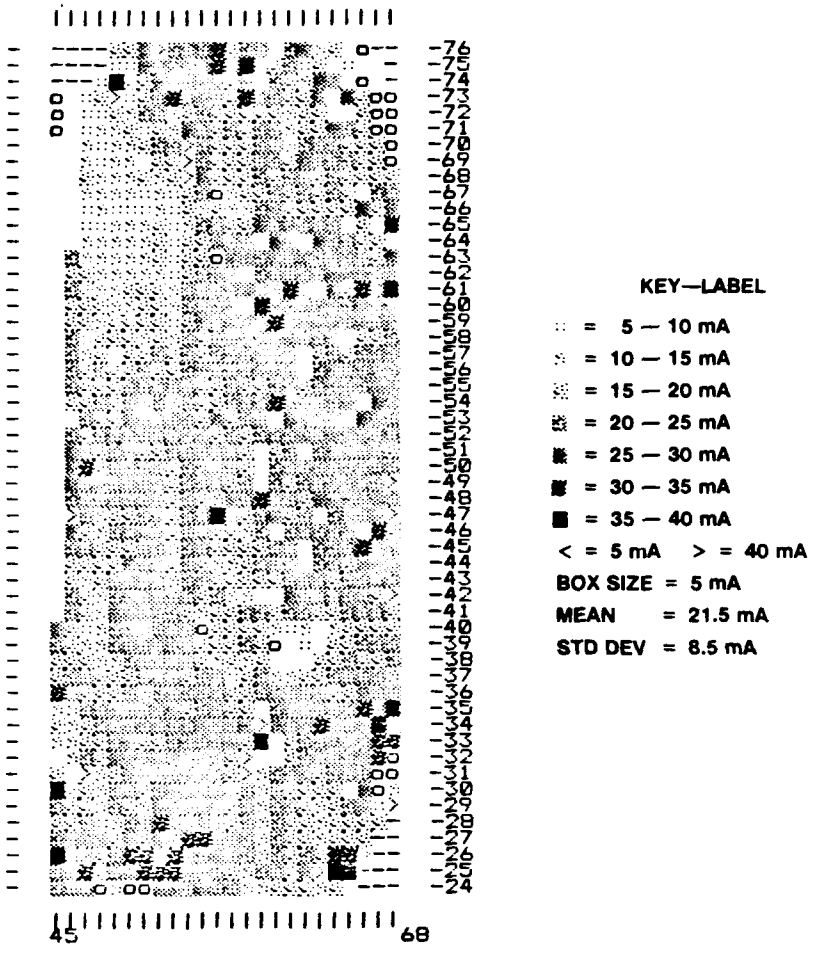


FIG 8 Map of saturated drain-source current in the range 5 to 40 mA, with zero gate voltage for wafer 10RO1/B.

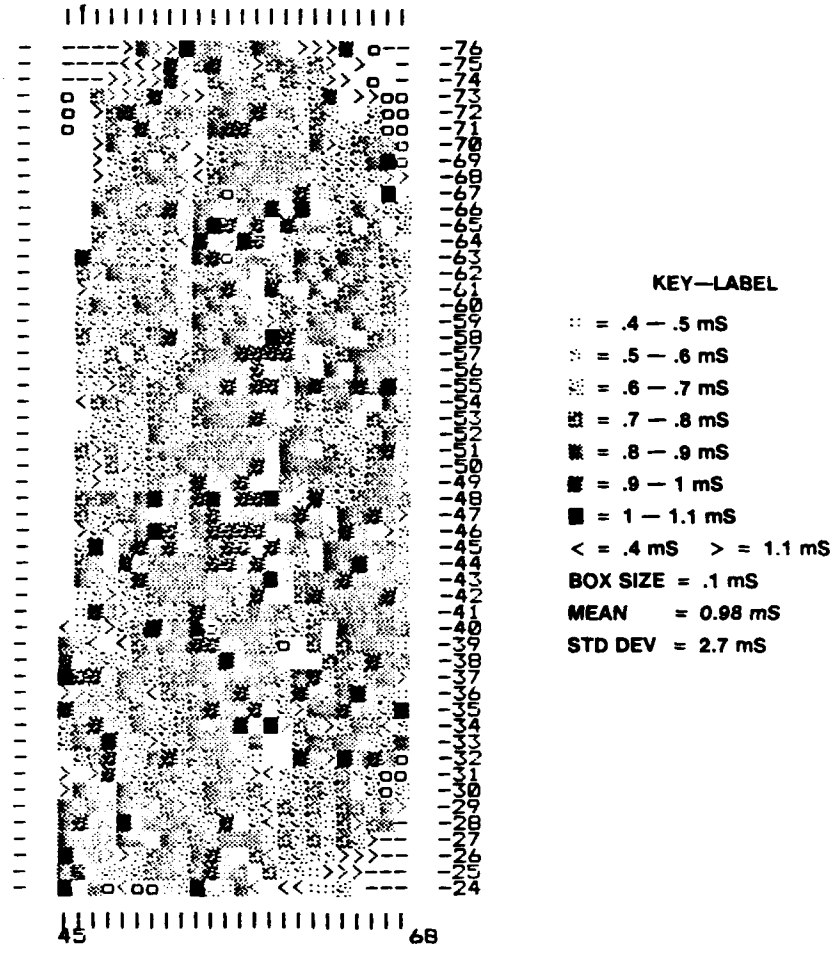


FIG 9 Map of output conductance in the range 0.4 to 1.1 mS for wafer 10RO1/B.

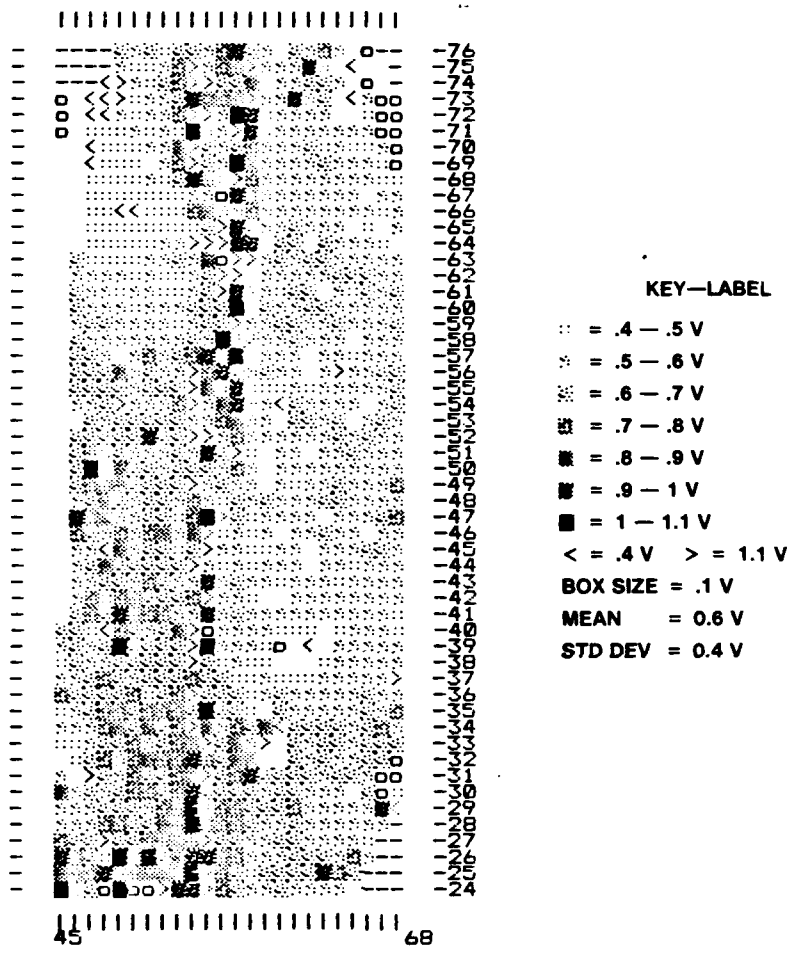


FIG 10 Map of knee voltage in the range 0.4 to 1.1 volt for wafer 10RO1/B.

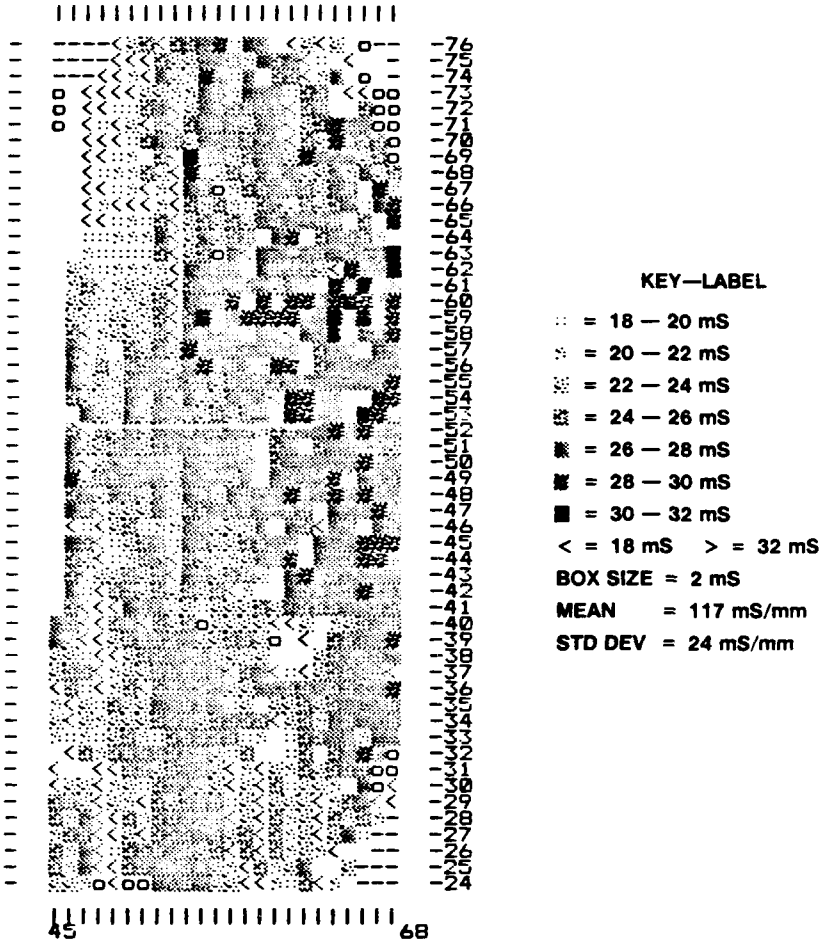


FIG 11 Map of forward transconductance in the range 18 to 32 mS per 200 μm gate width for wafer 10RO1/B.

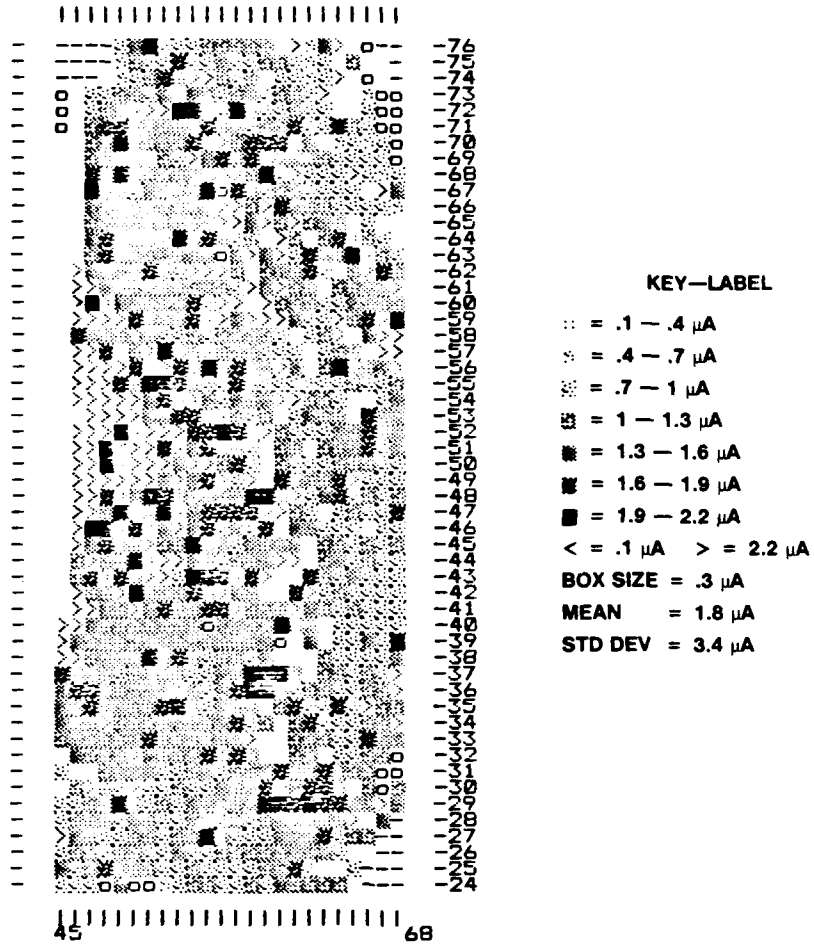


FIG 12 Map of gate leakage current in the range 0.1 to 2.2 μA with -4 volts gate bias and zero source-drain bias for wafer 10RO1/B.

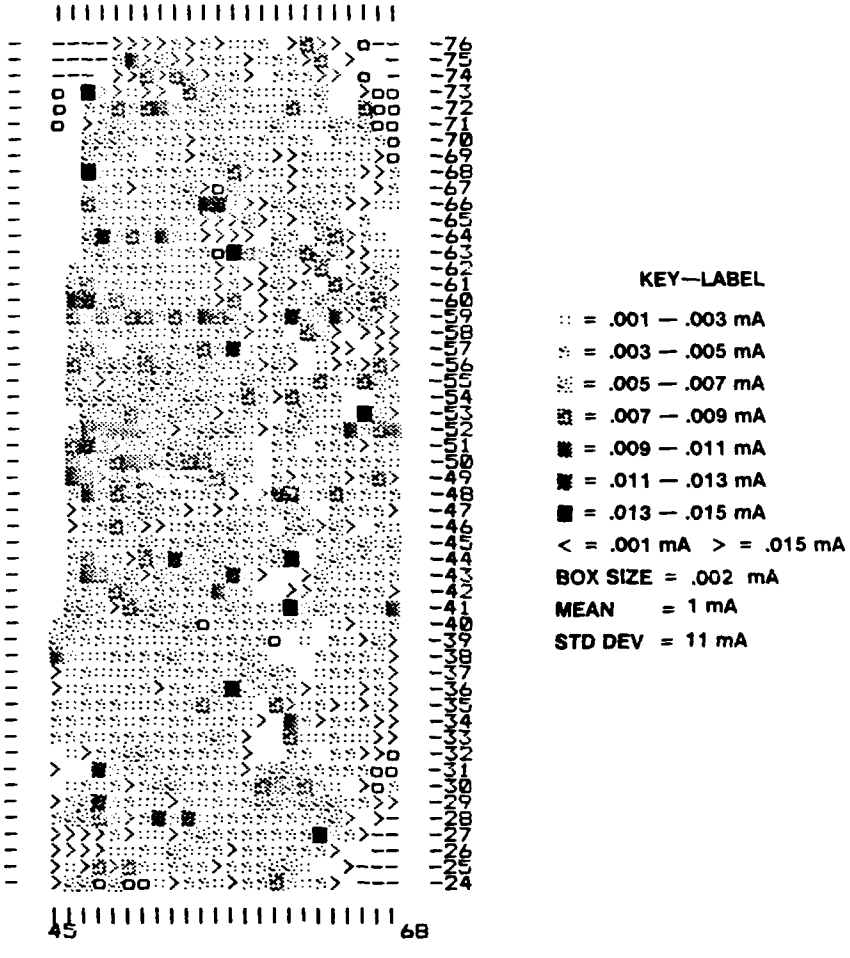


FIG 13 Map of drain-source current in the range 0.001 to 0.015 mA with -4 volts gate bias and 5 volts source-drain bias for wafer 10RO1/B.

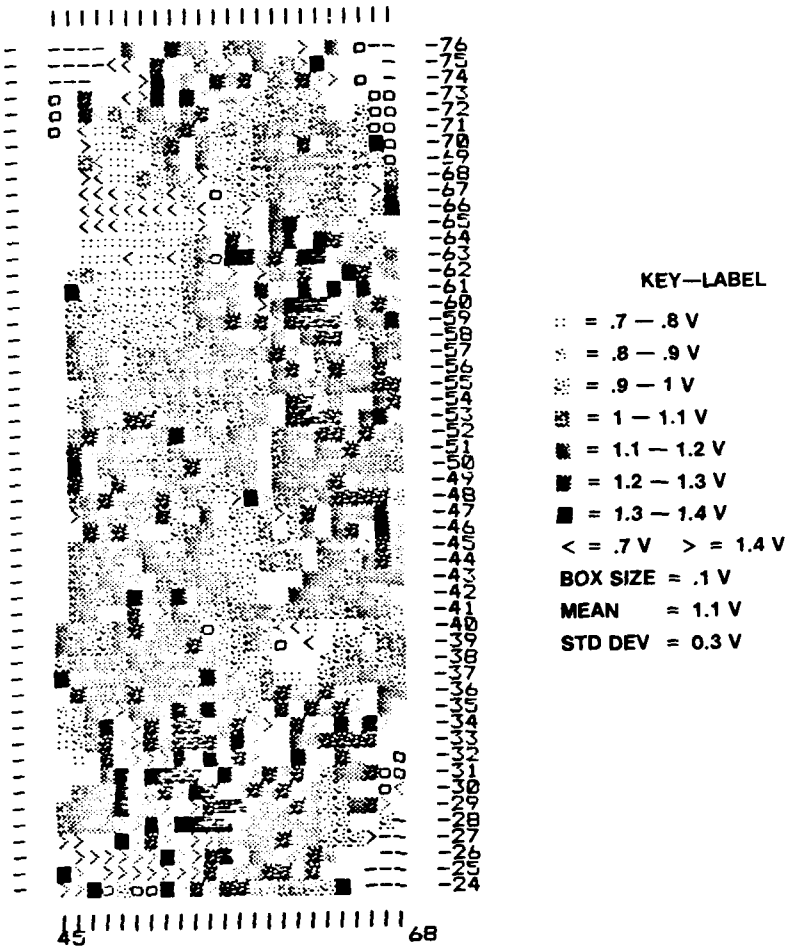
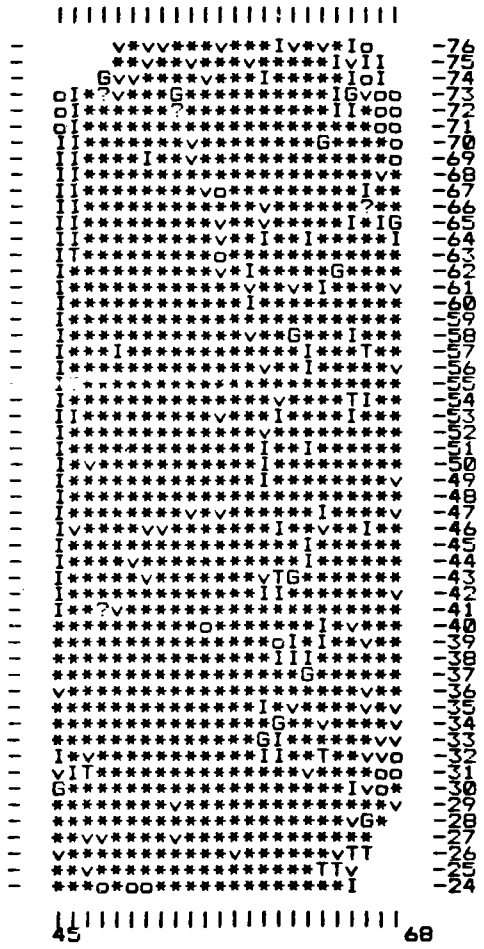


FIG 14 Map of pinch off voltage in the range 0.7 to 1.4 volts for drain-source current of 1 mA, at source-drain bias of 5 volts, for wafer 10RO1/B.



KEY—LABEL

*	=	1026 PASSES
		TOTAL NO. OF DEVICES = 1246
		YIELD = 82%
s	=	SHORT > 100 mA @ VDS 0.2 V
o	=	OPEN < .5 mA @ VDS 0.2 V
G	=	GATE I > 100 μA
T	=	Gm < .2 mS
R	=	RSLOPE > 500 OHM
v	=	VPINCH > 4 V @ 1 mA
I	=	IDSS0 > 200 mA
?	=	NULL DATA

FIG 15 Map of devices passing the limits, and identification of failure mode of failed devices, each device is uniquely numbered, wafer 10RO1/B.

SUMMARY OF PROCESSED WAFER DATA

WAFER NUMBER 38R03B

1. Processed by: EGB Start Date: 6.3.86 Finish Date: 1.4.86
2. Ion implantation: 7E12 at 240 keV + 7E13 at 90 keV, 7° tilt, 22° rotation, Silicon 29, through SiN_x.
3. Annealing: A_sH_3, 850°C for 20 min, face to face.
4. Mask set: CS - M534800 + Numbers.
5. Gate etch (seconds) 35 seconds - 1 step.
6. FET DC Data

Total number of Patterns = 816 X = 17 Y = 24 overall yield (%) = 76.

6A. Microwave (CSFET's) (default limits)

Parameter		mean	std dev.	display yield (%)
R_{slops}	[Ω]	24	9	97
I_{dsso}	[mA]	50	30	95
g_d	[mS]	1.9	0.5	85
V_{knee}	[V]	0.9	0.2	85
g_m	[mS]	22	2	85
I_{gate}	[μA]	1	4	85
I_{dss4}	[mA]	0.9	4	85
V_p	[V]	2.5	0.6	76

6B. Standard FET'S (orthogonal)

Parameter		Left hand side			Right hand side		
		mean	st. dev	yield (%)	mean	std. dev	yield
R_{slope}	[Ω]	39	8	97	40	10	98
I_{dsso}	[mA]	30	20	97	30	10	98
g_d	[mS]	0.5	0.5	90	0.4	0.3	95
V_{knee}	[V]	1.0	0.1	90	0.9	0.1	95
g_m	[mS]	12	2	90	12	2	95
I_{gate}	[μA]	9	10	89	9	10	94
I_{dss4}	[mA]	2	7	89	1	4	94
V_p	[V]	2.6	0.6	74	2.6	0.6	80

Fig 16A - LOGGING OF WAFER DATA (D.C)

8. RF Data f = 9.0 GHz Number of Devices = 13

		selected mean	selected st. dev.	Random mean	Random st. dev
MAG [dB]	S_{11}			0.54	0.02
	S_{12}			0.051	0.007
	S_{21}			1.3	0.1
	S_{22}			0.78	0.02
PHASE [o]	S_{11}			-160	20
	S_{12}			63	8
	S_{21}			46	6
	S_{22}			-46	4

Selection Definition: only d.c acceptance limits

9. Equivalent Circuit Parameters Number of devices = 13

Parameter		mean	std. Dev.
L_g	[nH]	0.5	0.1
R_g	[Ω]	0.05	0
C_{gs}	[pF]	0.52	0.06
R_i	[Ω]	10	4
C_{gd}	[fF]	17	2
g_m	[mS]	28	2
Tau	[pS]	7.0	0.8
C_{ds}	[pF]	0.12	0.01
R_{ds}	[Ω]	620	60
R_d	[Ω]	10.0	0.5
L_d	[nH]	0.27	0.02
R_s	[Ω]	10	1
L_s	[nH]	0.081	0.005

Selection Definition: only d.c acceptance limits

10. Bonding Comments

11. Amplifier Comments

Fig 16B - LOGGING OF WAFER DATA (RF)

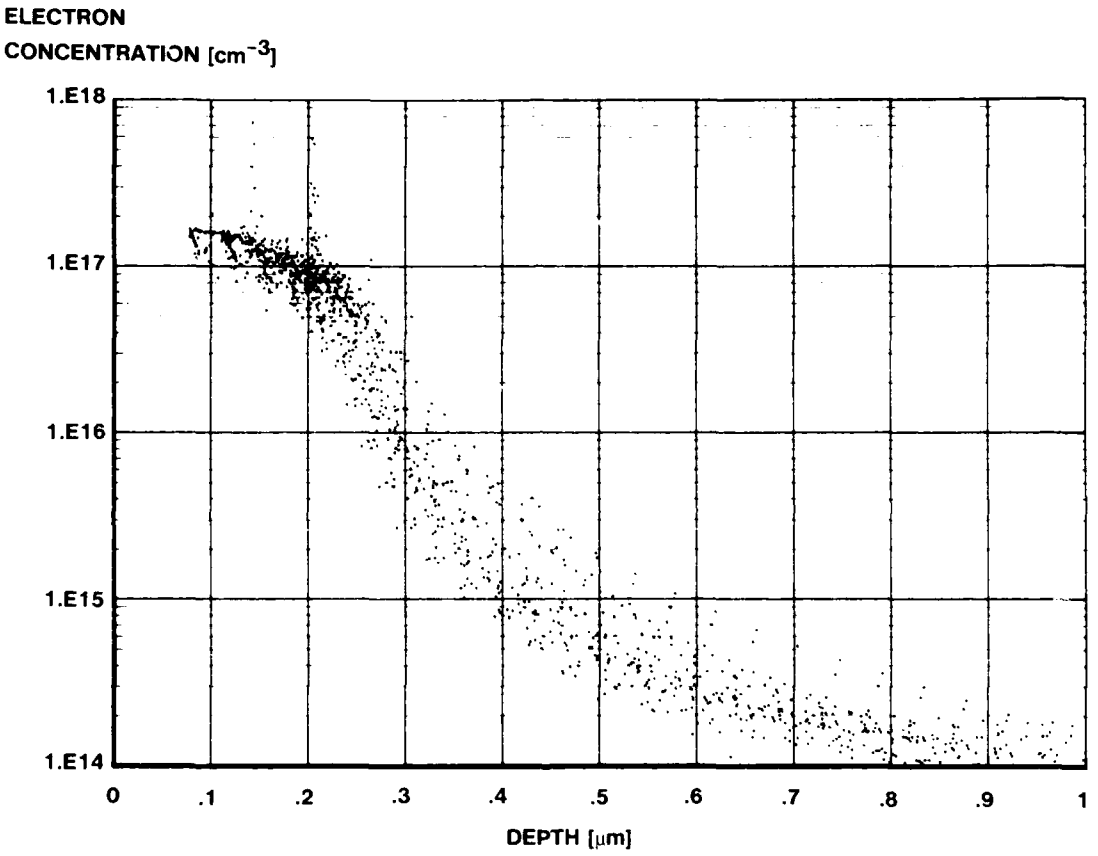


FIG 17 ELECTRON CONCENTRATION - DEPTH PROFILES OBTAINED BY C-V PROFILING OF FATFETS.

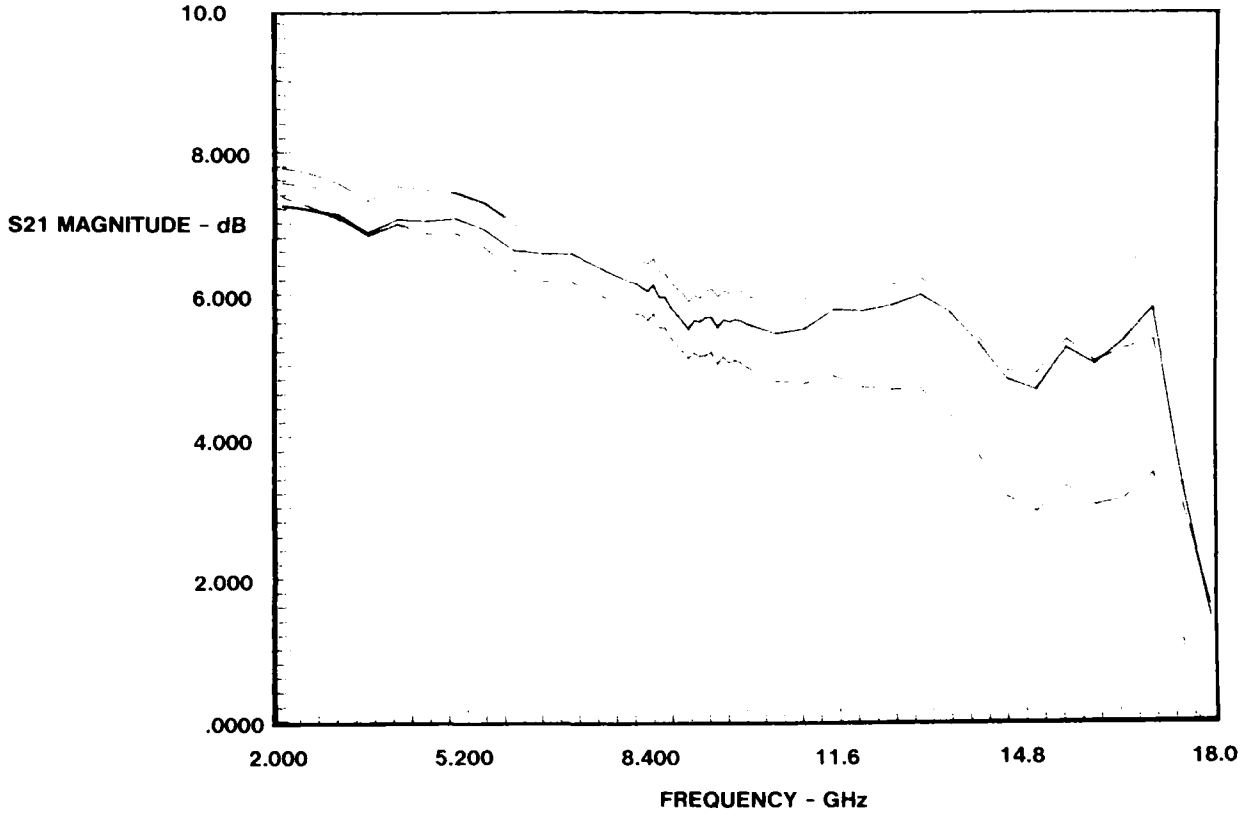


FIG 18 FORWARD GAIN VERSUS FREQUENCY FOR 6 RANDOMLY SELECTED FETS FROM WAFER 10R01/A

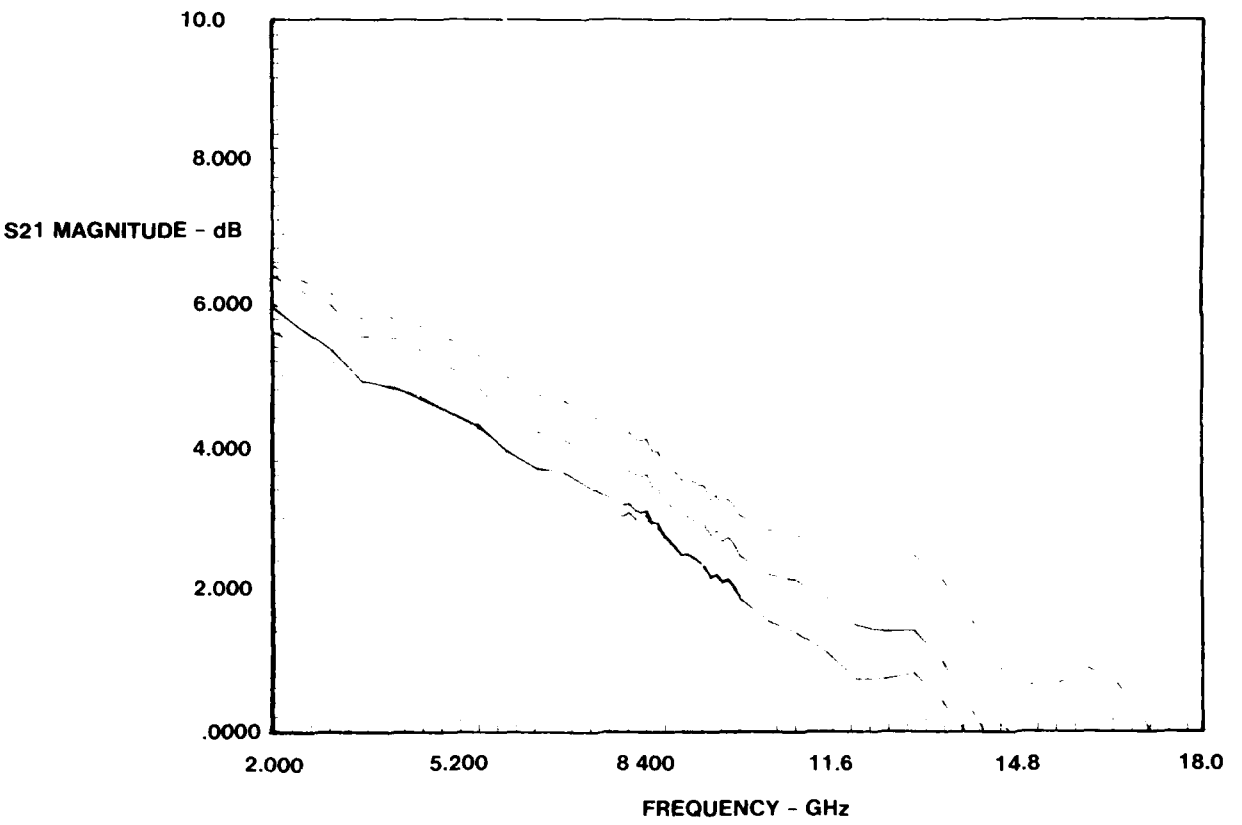


FIG 19 FORWARD GAIN VERSUS FREQUENCY FOR 6 RANDOMLY SELECTED FETS FROM WAFER 38R03/B

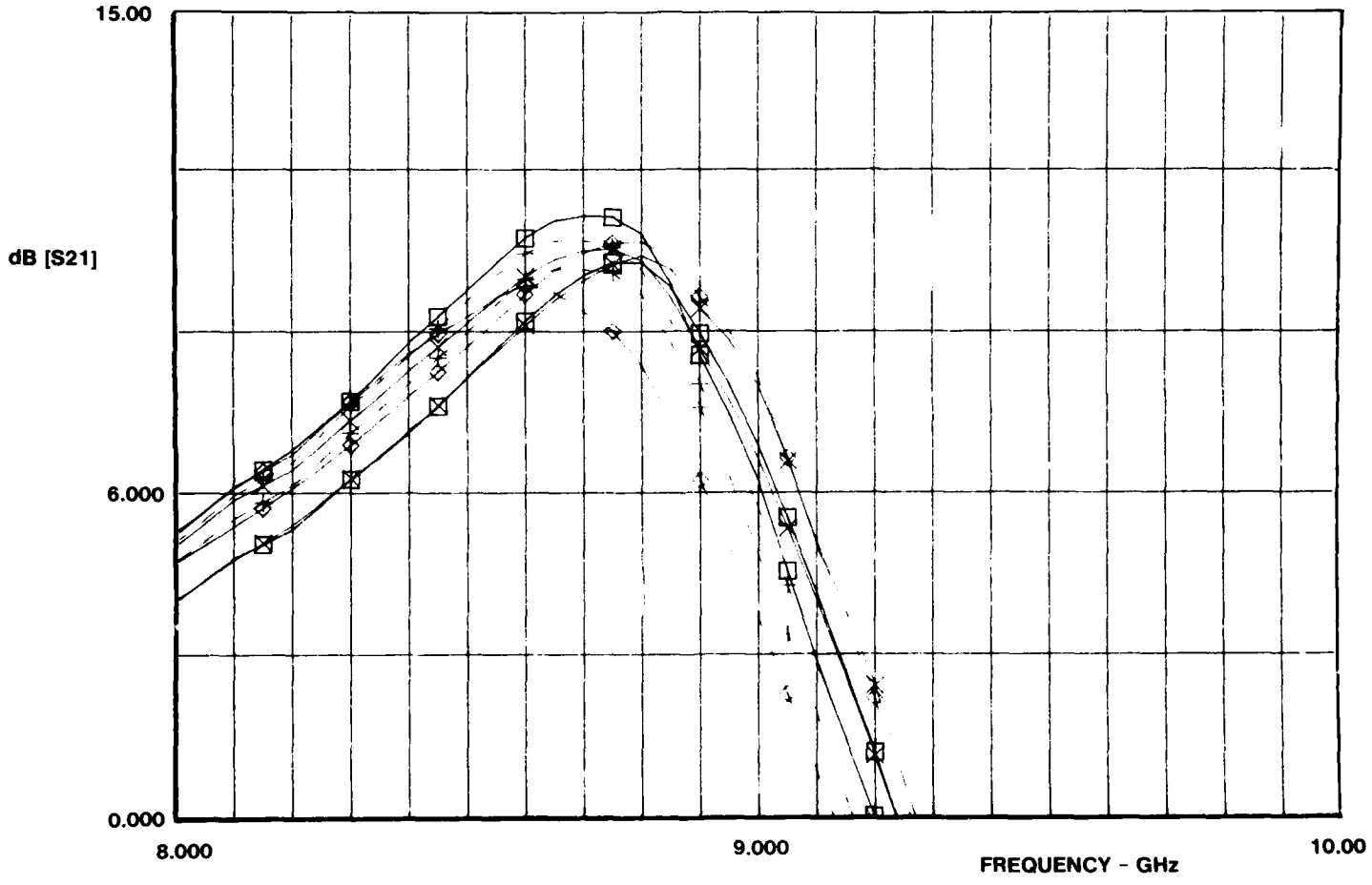


FIG 20 THE PREDICTED AMPLIFIER GAIN VERSUS FREQUENCY FOR 8 FETS, WITH SELECTION CRITERIA OF gm IN THE RANGE OF 20 TO 25 mS.

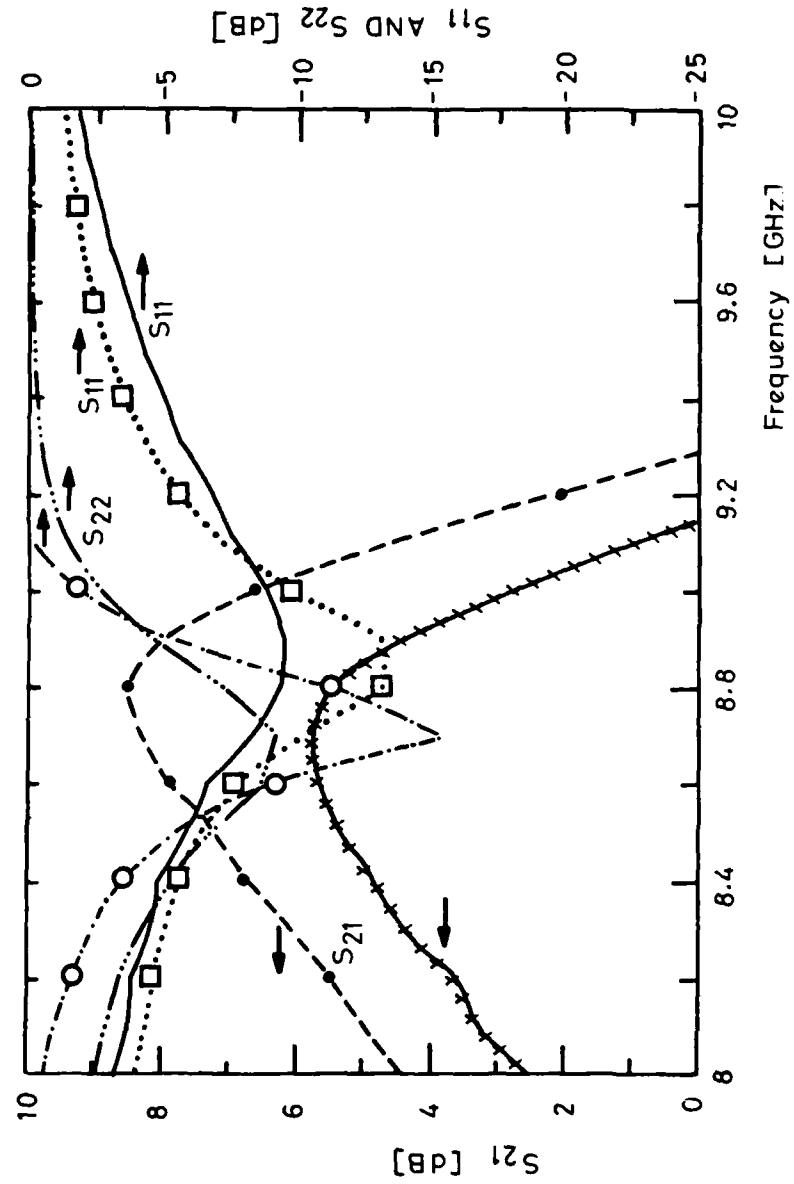


FIG 21 Comparison of predicted and measured r.f. performance of the amplifier in the frequency range 8 to 10 GHz;

S_{21}: — — • — — (measured), x x x x (predicted);

S_{11}: · · · · □ · · · · (measured), —— (predicted)

S_{22}: — · — ○ — · — (measured), —— · · · —— (predicted).

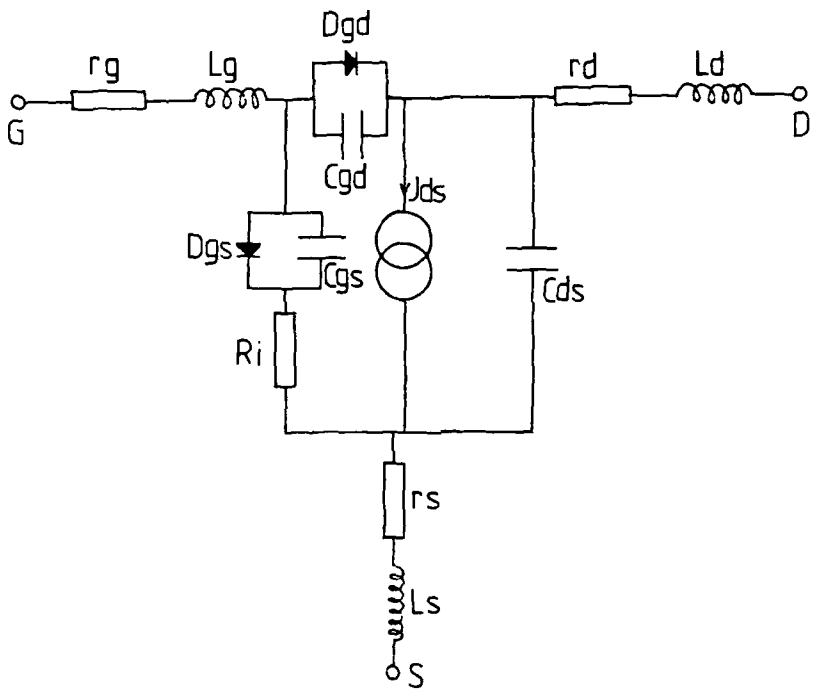


FIG 22 Large signal equivalent circuit of GaAs MESFET.

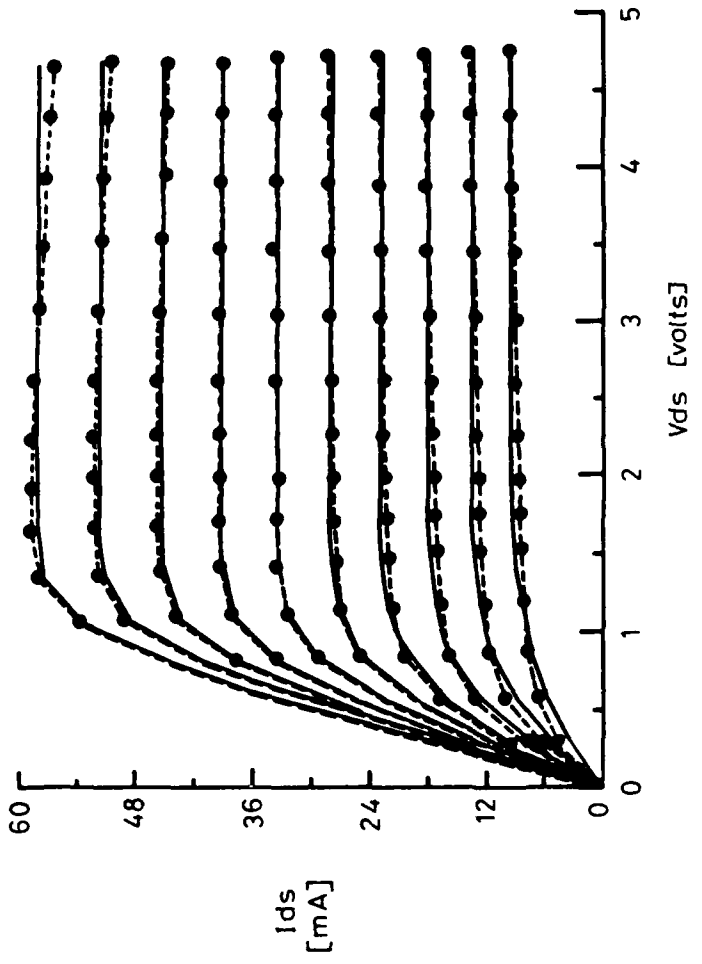


FIG 23 The measured (—•— —•—) and predicted (——) I_{ds} - V_{ds} characteristics of FET 04RO5/41.14.

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	Memo 4164		U/C

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ION IMPLANTED GaAs MICROWAVE FETs

7a. Title in Foreign Language (in the case of translations)

7b. Presented at (for conference papers) Title, place and date of conference

8. Author 1 Surname, initials	9(a) Author 2	9(b) Authors 3,4...	10. Date	pp. ref.
GILL, S.S.	BLOCKLEY, E.G.	DAWSEY, J.R. et al	1988	VP

11. Contract Number	12. Period	13. Project	14. Other Reference

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Abstract The combination of ion implantation and photolithographic patterning techniques has been applied to the fabrication of GaAs microwave FETs. This approach was adopted with the aim of providing a large number of devices having consistently predictable d.c. and high frequency characteristics. This memorandum concentrates on a description of the technology research carried out between 1983 and 1986 which culminated in the successful demonstration of a processing scheme meeting this objective. To validate the accuracy and repeatability of the high frequency device parameters, an X-band microwave circuit has been designed and realised. The performance of this circuit, a buffered amplifier, was very close to the design specification. The availability of a large number of reproducible, well-characterised transistors has enabled work to commence on the development of a large signal model for FETs. The preliminary work in this area is also described in this report.

As a consequence of this research programme on ion implanted GaAs FETs, considerable advances have been made in the areas of process control, d.c. and rf characterisation, and modelling techniques. All of these topics are important elements in future research at RSRE in microwave devices and circuits.